CONNECT
COLLABORATE
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# NSF Workshop on Research Education and Workforce Development

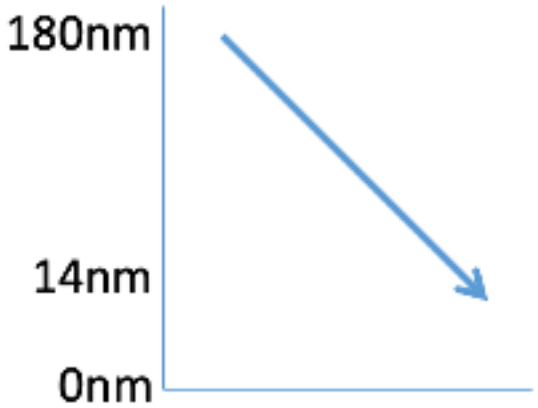
October 14/15, 2021

**Mohamed Kassem**

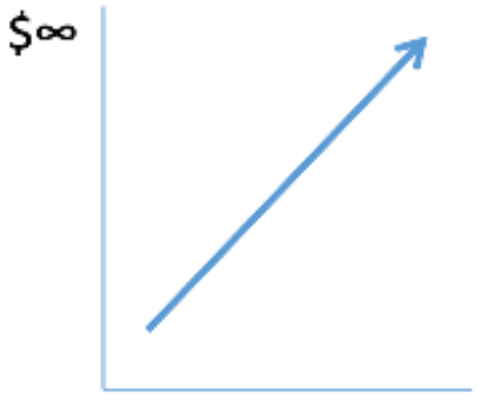
Cofounder & CTO, EFABLESS.COM

mkk@efabless.com

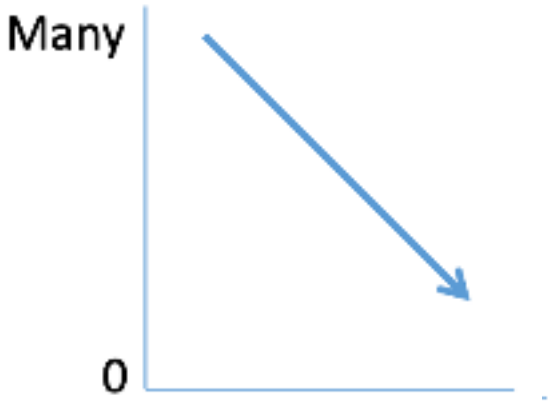
# CHALLENGING INDUSTRY TRENDS



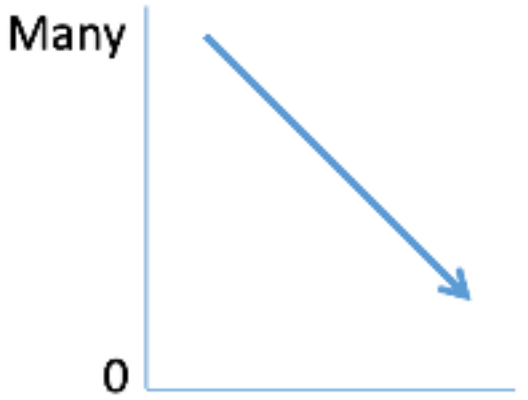

As Transistor Size Goes To Zero




Development Cost Goes to Infinity




Number of Customers Goes to Zero

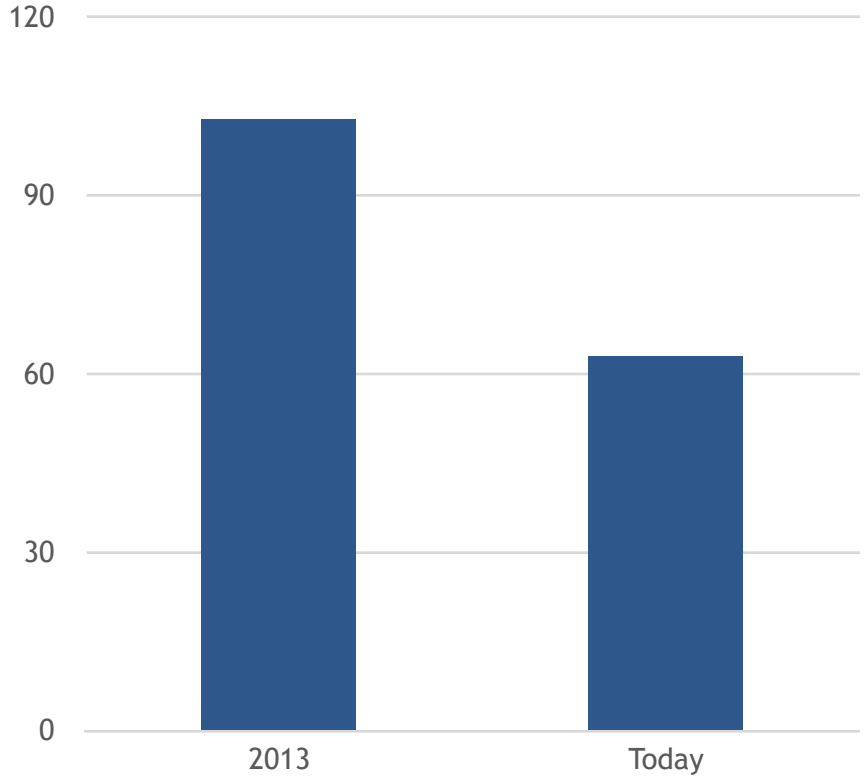



Number of Designers Goes to Zero

Source: Mike Noonen

# INDUSTRY DYNAMICS

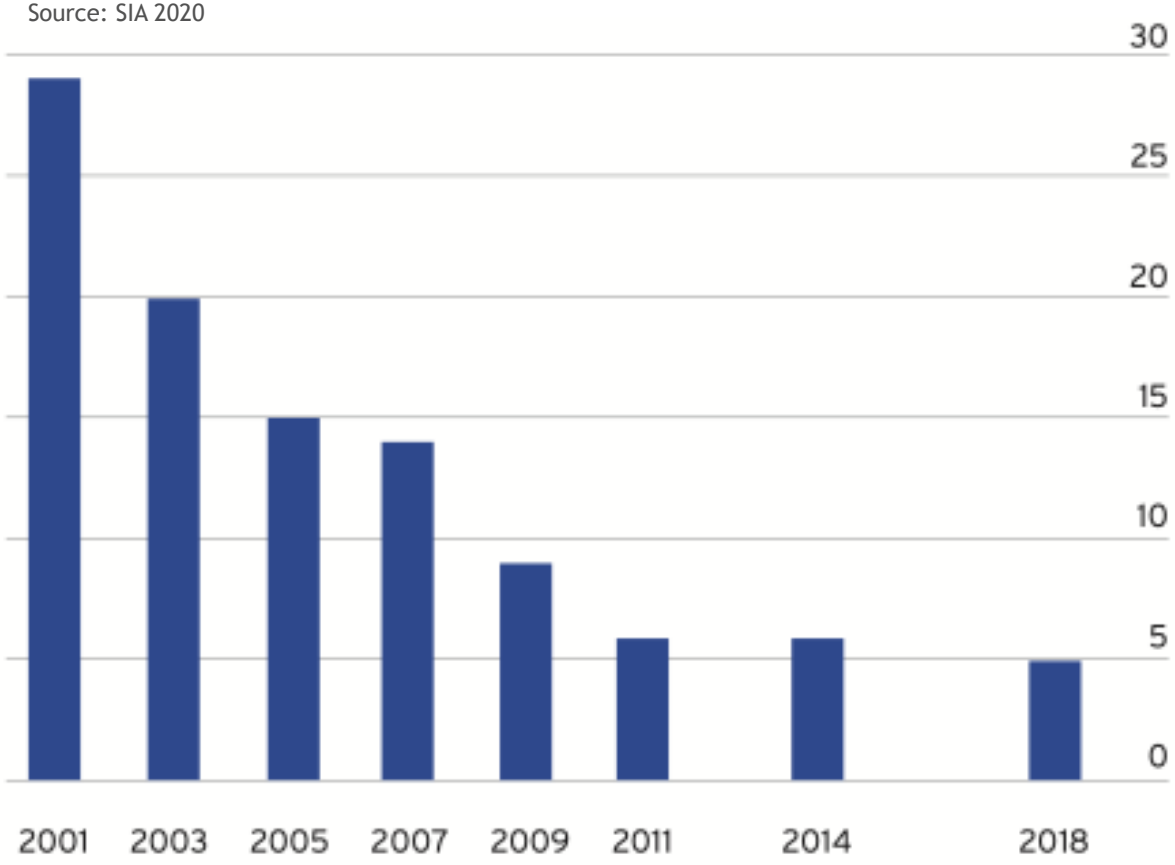
Source: Morgan Stanley




Semiconductor industry consolidation

## Semi Companies Larger Than $100M

Source: SIA 2020




## Semi Companies Delivering Lead-in Edge Tech



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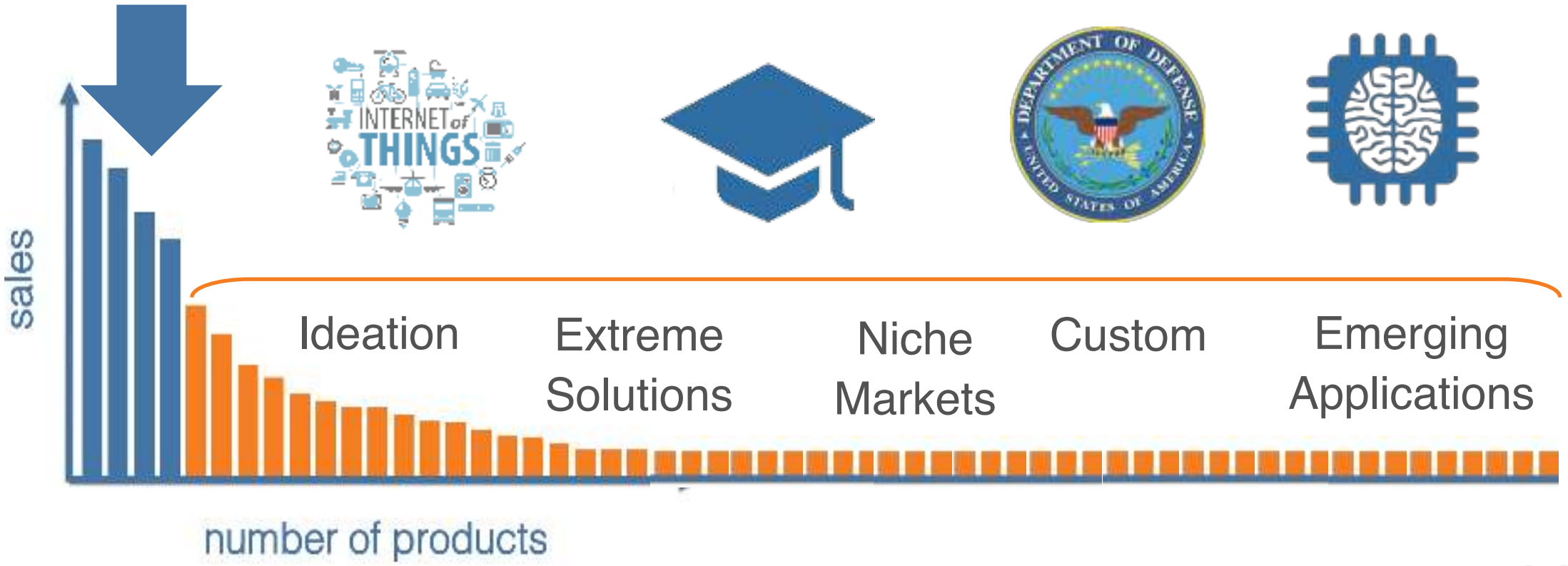
# THE FUTURE - THE DESIGN GAP

**Markets Served By Traditional Methodology**

**LONG TAIL INNOVATION REQUIRED!!**
**On A Massive Scale**
**10,000's of Products**



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# THE TALENT GAP

***Is the industry concerned about innovation in semiconductors & its applications? ….Yes!***


*John Neuffer, CEO of SIA, at GlobalFoundries GTC2020 Forum*

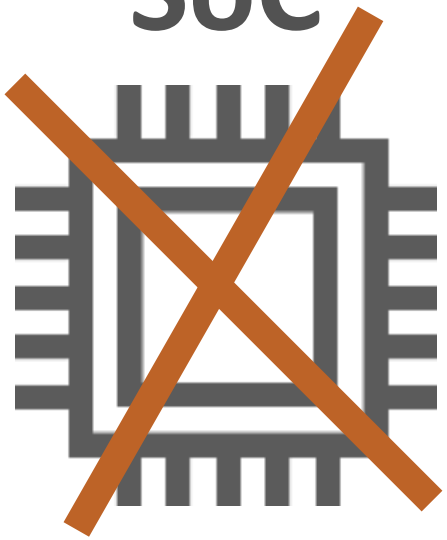
# CURRENT CHALLENGES IT'S AN AND GATE

1. Market Needs
2. Multidiscipline Knowledge
3. IP
4. EDA Tools
5. PDK
6. AFFORDABLE MFG/ASSY/TEST

AND

***Real** life application*

SoC





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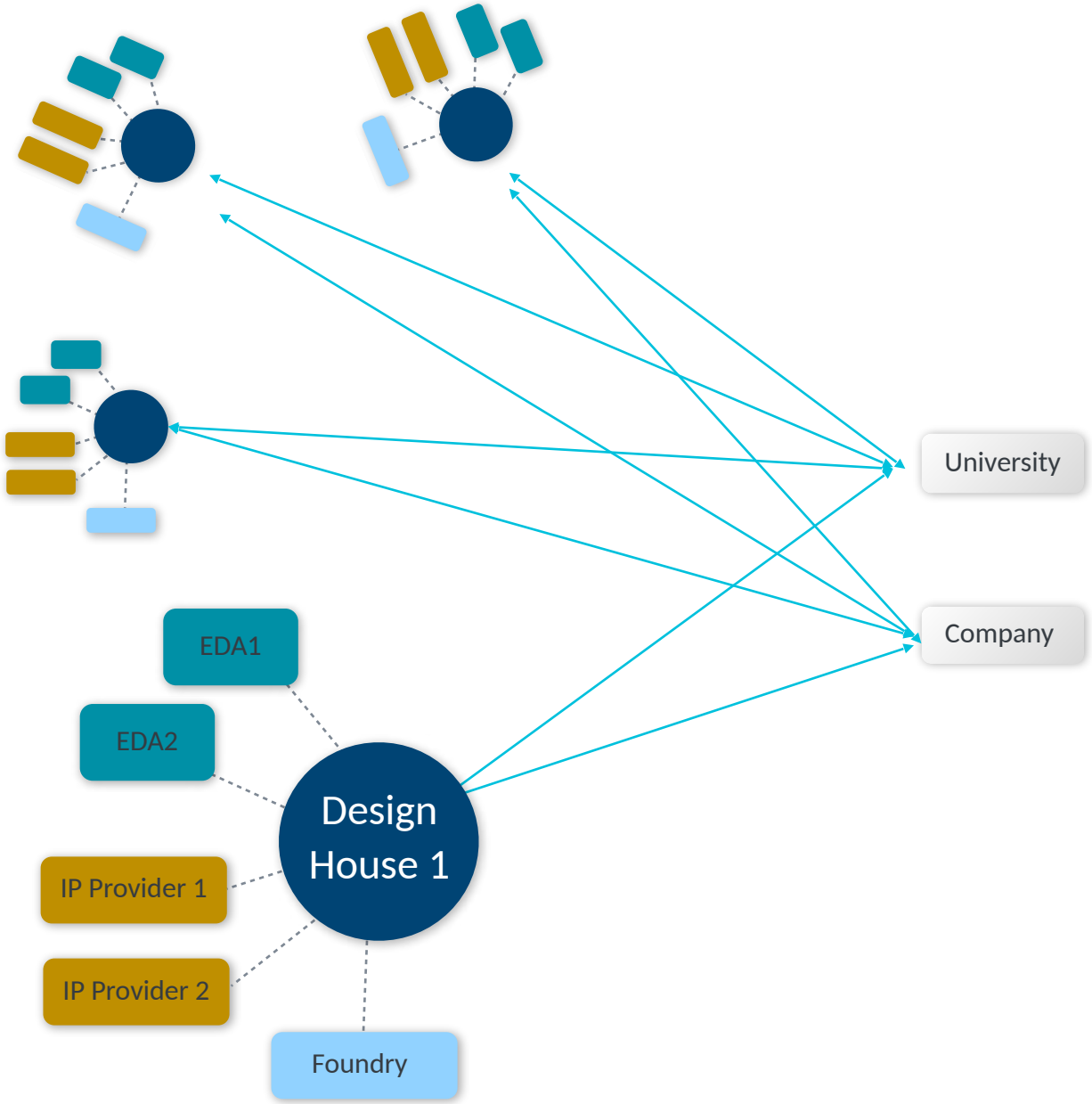
# TODAY'S APPROACH




Every design entity needs to establish **independent** business and contractual (including NDA's) relationships with **multiple** IP providers, EDA vendors, and foundries



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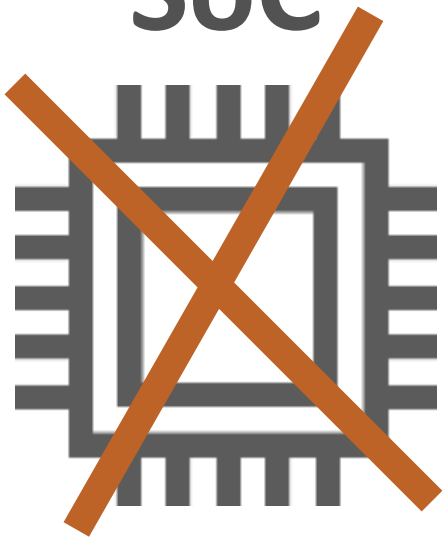
# PARTIAL SOLUTIONS FAIL

1. Market Needs
2. Multidiscipline Knowledge
3. IP
4. EDA Tools
5. PDK
6. AFFORDABLE MFG/ASSY/TEST

AND

***Real** life application*

SoC





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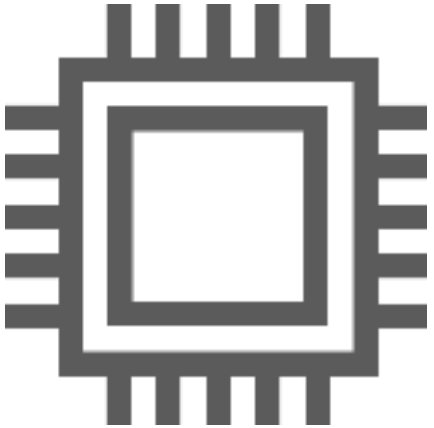
# MUST CREATE NO COMPROMISE CHANGE

1. Market Needs
2. Multidiscipline Knowledge
3. IP
4. EDA Tools
5. PDK
6. AFFORDABLE MFG/ASSY/TEST

AND

***Real** life application*

**SoC**





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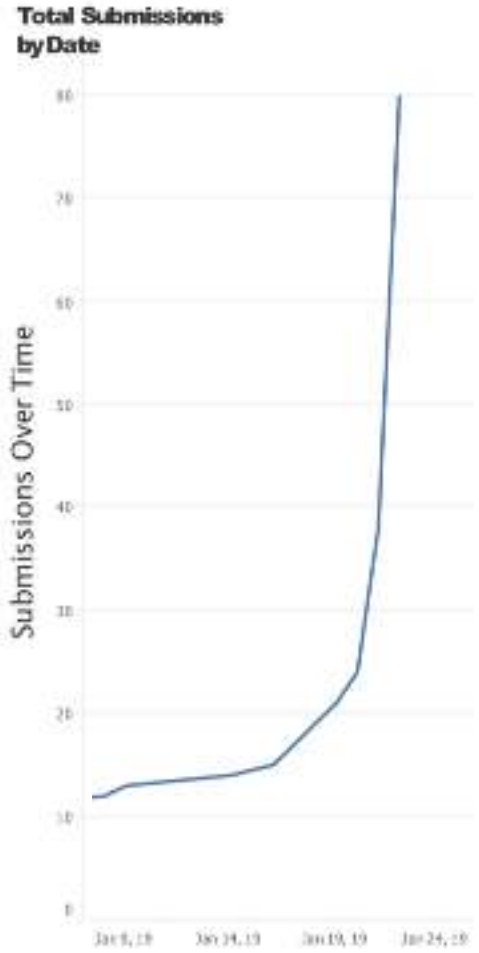
# GOV'T SUPPORT EXAMPLE


## AFRL's Advanced Microelectronics Design & Prototype Challenge

What is your solution for a **14/12nm** advanced SoC that can operate and improve the features of an **autonomous** product of your choosing while **maintaining** the **integrity** (provenance, traceability) and **security** needs (information protection, mathematical algorithms) of critical systems?

# ME CHALLENGE STATS


**82** TOTAL SUBMISSIONS

**45** SHOWCASE INVITEES

**12** PHASE1 FINALISTS

**3** PHASE2 FINALISTS

## Link to the Proposals

https://drive.google.com/drive/folders/1lyVPkLx1vpWcK8R-KJIgX42zdbRSeBBh?usp=sharing

# AFRL CHALLENGE — KEY OBSERVATIONS

- **No shortage of ideas** / target applications
- When you eliminate the barriers - **Talent shows up**
- **Size ranges from 2-person to 50+ person entities**
- Many of the performers newly exposed to 12nm node
- Because it was public - **facilitated collaboration work**
- 7-month delay dose of licensing & contractual gates

# WHAT EFABLESS DOES

**simplify Chip creation** and

open **it to everyone**



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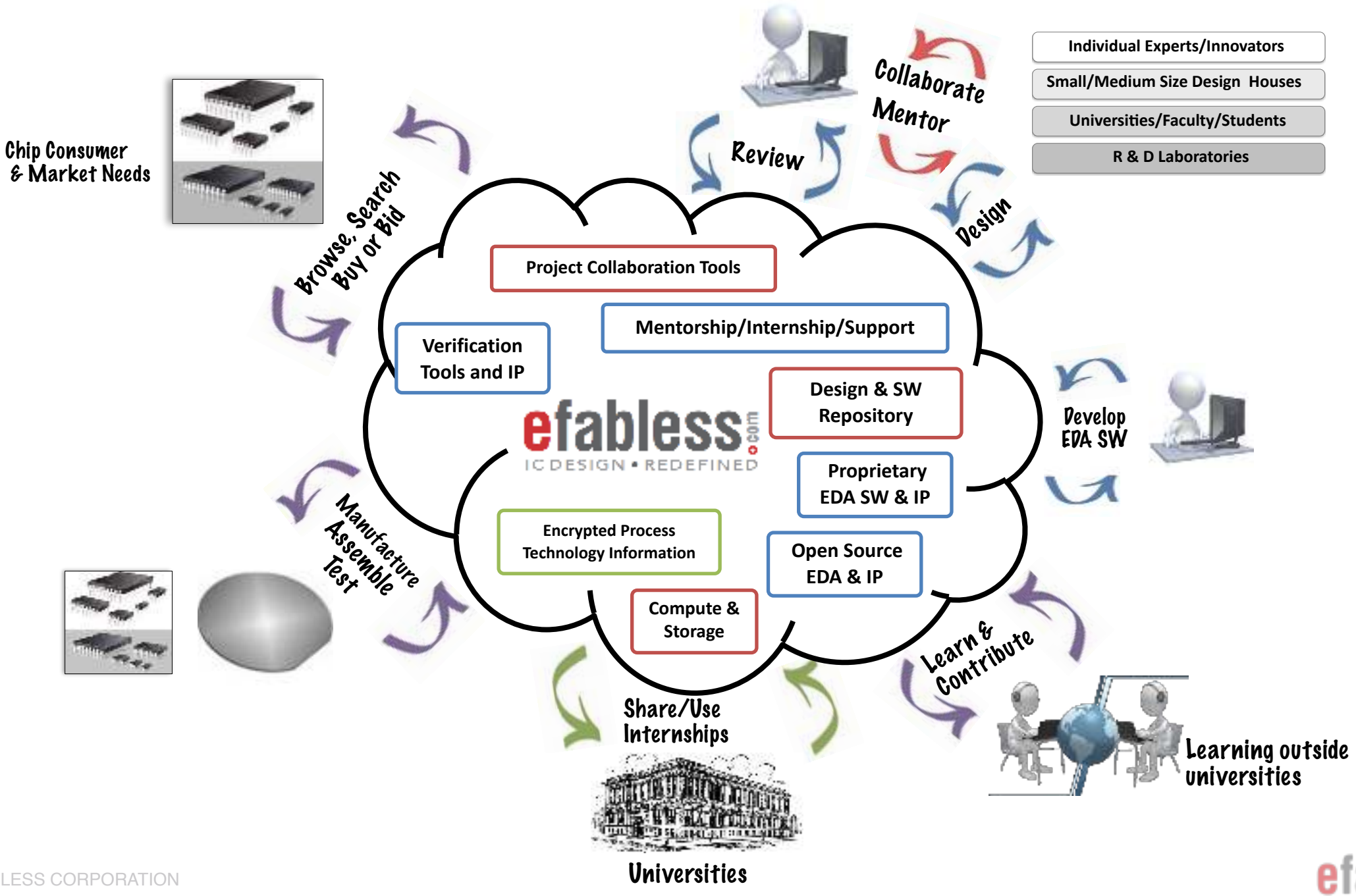


# CLOUD - BUT NOT FOR COMPUTE

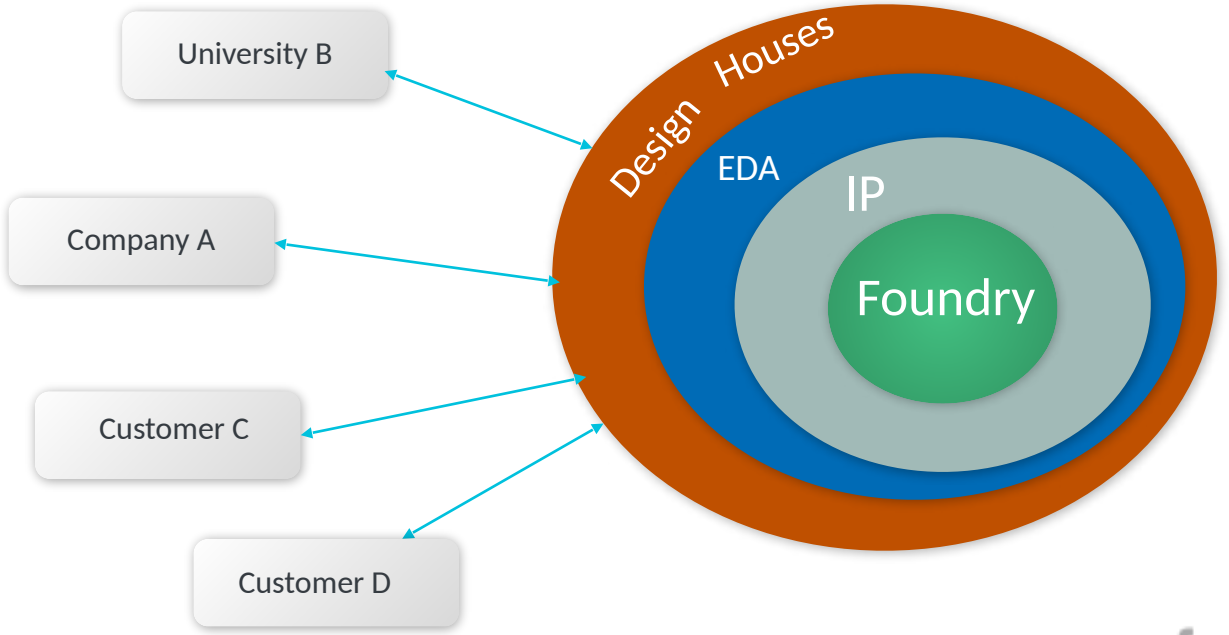
Secure, cloud-based platforms, all the resources and processes required to design ASICs and IP are offered in one place while maintaining the “fire-walling" of IP information and with enhanced traceability and on-demand elasticity.

Enabling a worldwide network of developers and customers to collaborate, model, and verify custom SoCs. When custom SoC creation becomes less risky and more cost-effective, innovation is unleashed.

Scalable & elastic design/development capacity

Facilitates Collaboration, reference designs and design re-use accelerates development and reducing costs

Risk reward sharing enabled by consolidated contribution tracking and design obfuscation



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# FOUNDRY DATA OBFUSCATION

Mask-geometry layout is foundry proprietary.

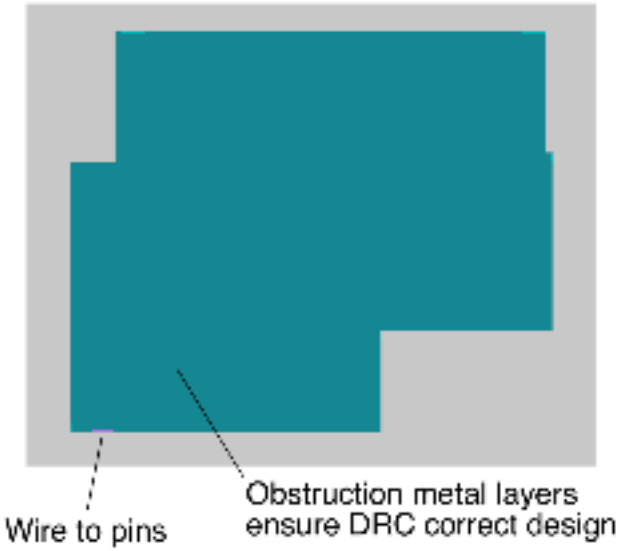
How can you design an entire chip and submit to the foundry for fabrication without signing an NDA, purchasing commercial tools, and installing PDKs?

All analog cells at the transistor level are abstracted views using information from the corresponding LEF files and simulation models

3.3V ADC, Original vendor layout:

(Layout blurred to protect the identity of the victim)

3.3V ADC, Abstracted layout (from LEF view):



# DESIGN IP OBFUSCATION

The target process: **X-FAB XH018**

Base MOS LP (low power) option

6 metal stack (5 standard route layers, 1 thicker top

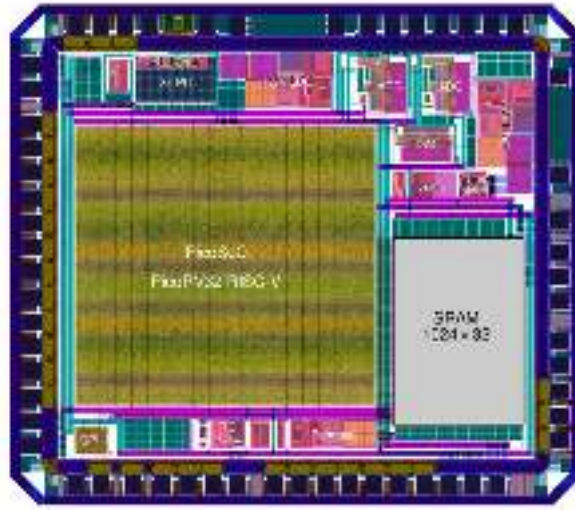
The proprietary data:

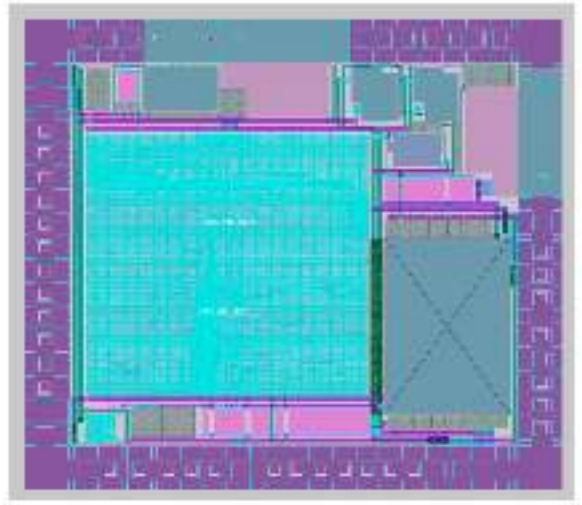
X-FAB digital standard cells

X-FAB I/O Cells(3.3V with both 3.3V and 1.8V core)

X-FAB Analog IP

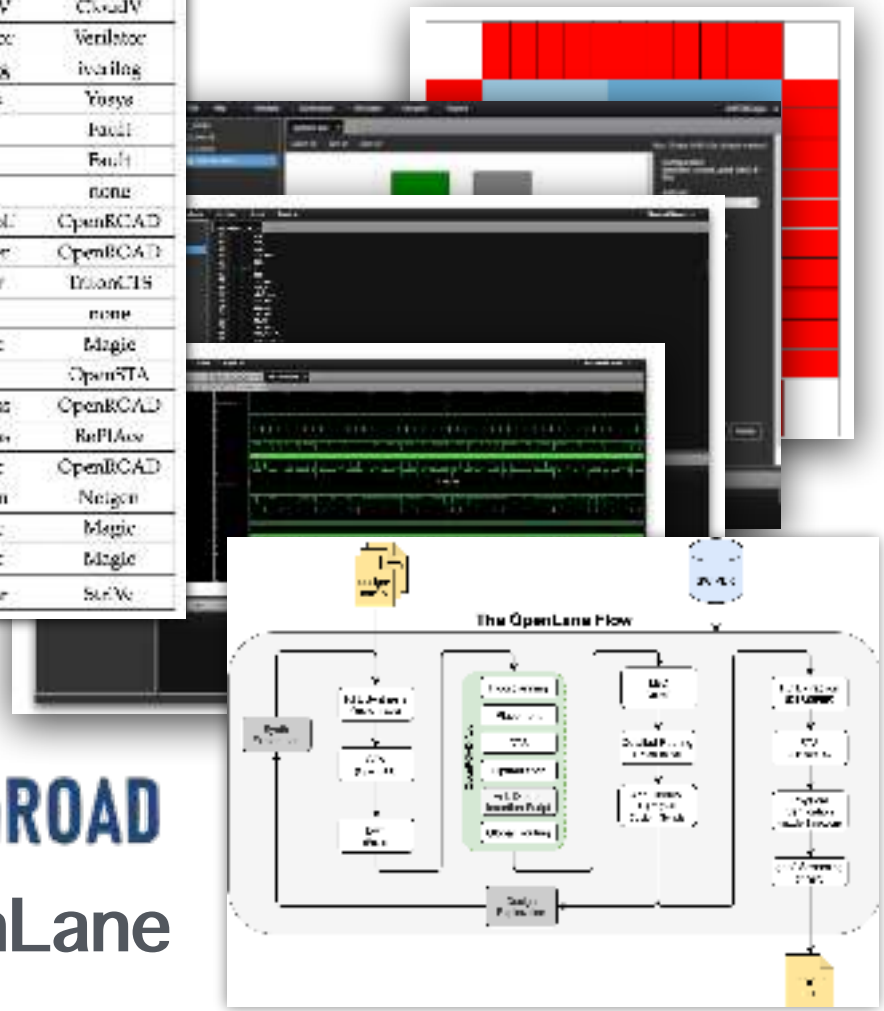
X-FAB SRAM (from memory compiler)





# OPEN SoC DESIGN FLOWS & TOOLS

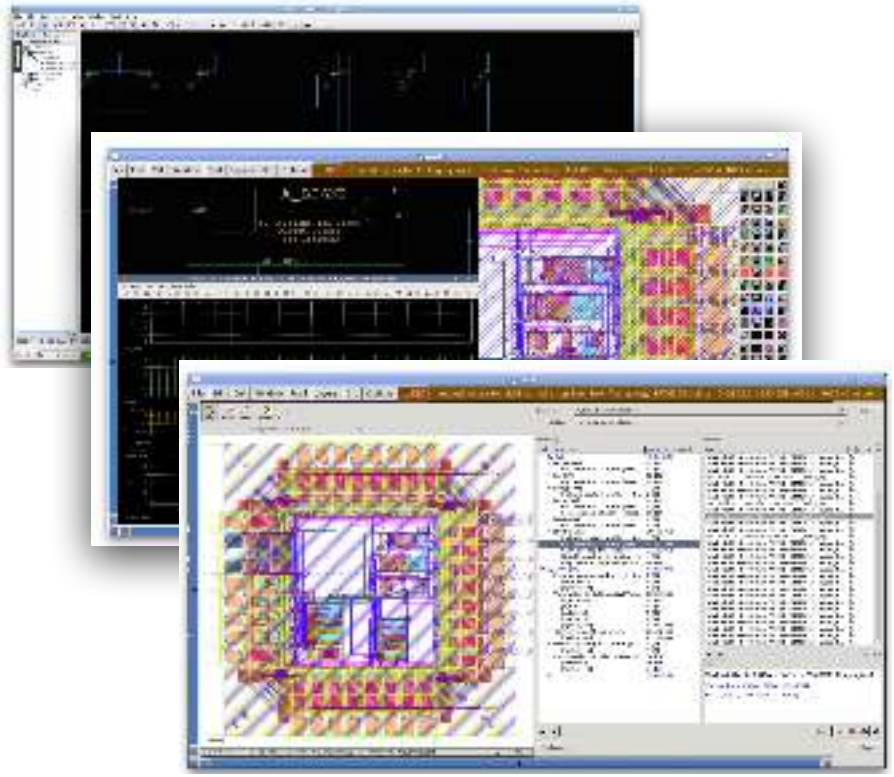
| DESIGN STEP | Qflow | CloudV SoC | OpenLane |
|---|---|---|---|
| System Design | N/A | CloudV | CloudV |
| RTL Lint | Verilator | Verilator | Verilator |
| RTL Simulation | Iverilog | Iverilog | iverilog |
| Logic Synthesis | Yosys | Yosys | Yosys |
| DFT Scan Insertion | none | none | Fault |
| DFT ATPG | none | none | Fault |
| Formal Verification | none | none | none |
| Placement | graywolf | graywolf | OpenRCAD |
| Routing | qrouter | qrouter | OpenRCAD |
| CTS | Qflow | Qflow | TritonCTS |
| Dynamic IR/EM | none | none | none |
| Extraction | Magic | Magic | Magic |
| Timing Analysis | Vesta | Vesta | OpenSTA |
| Floorplanning | Magic | efabless | OpenRCAD |
| Top-Level Placement | Magic | efabless | RePlAce |
| Top-Level Routing | Magic | Magic | OpenRCAD |
| LVS | Netgen | Netgen | Netgen |
| DRC | Magic | Magic | Magic |
| GDS | Magic | Magic | Magic |
| SoC | Raven | Raptor | SoC Vc |




- SoC Editor
- RTL Simulation
- Synthesis
- GL Simulation

OpenROAD

OpenLane



- Schematic Capture
- SPICE Simulation

- Mixed-Mode Simulation
- Parasitic Extraction
- Physical Verification



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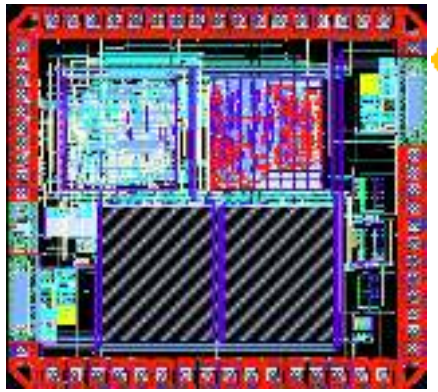
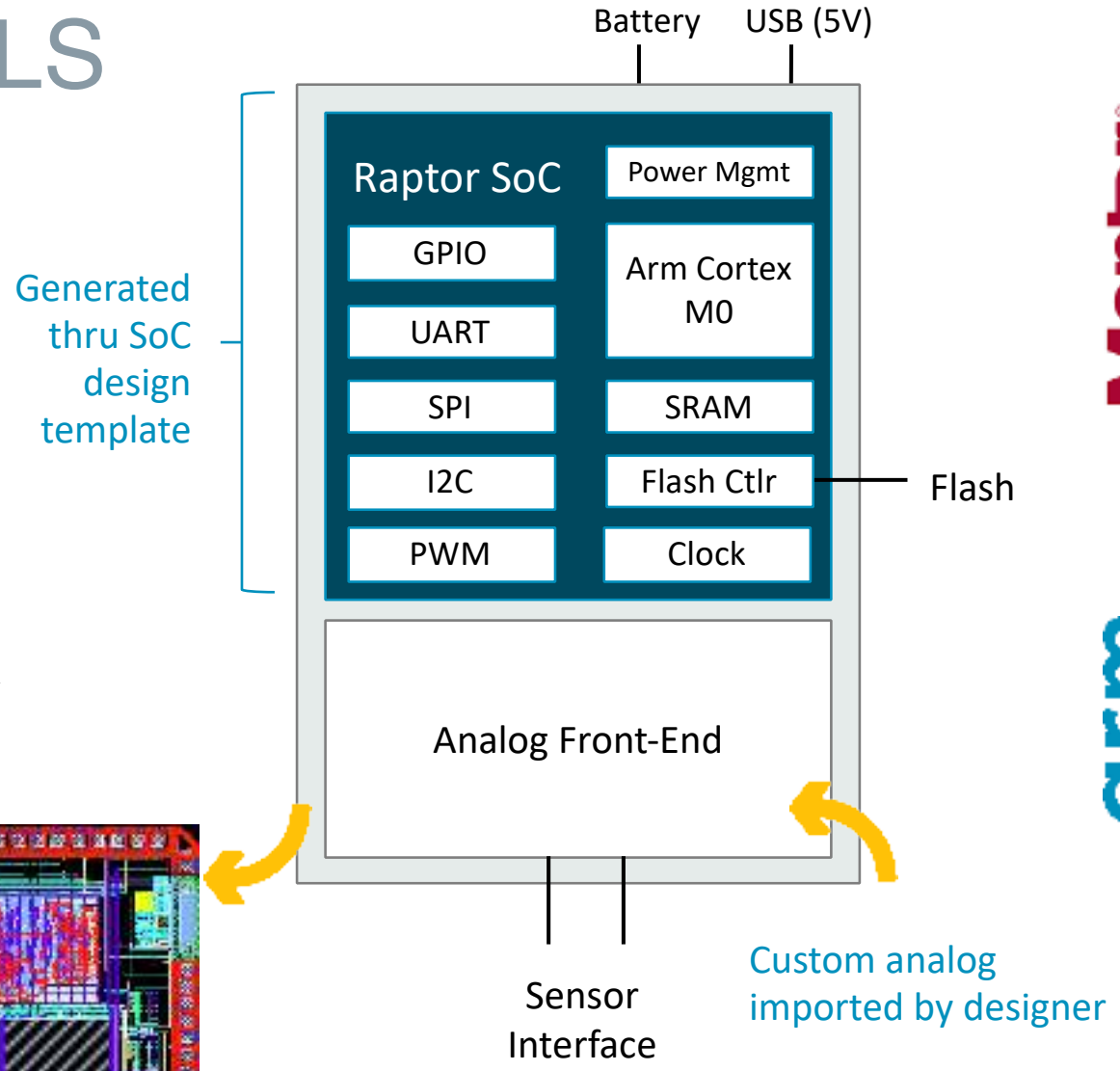
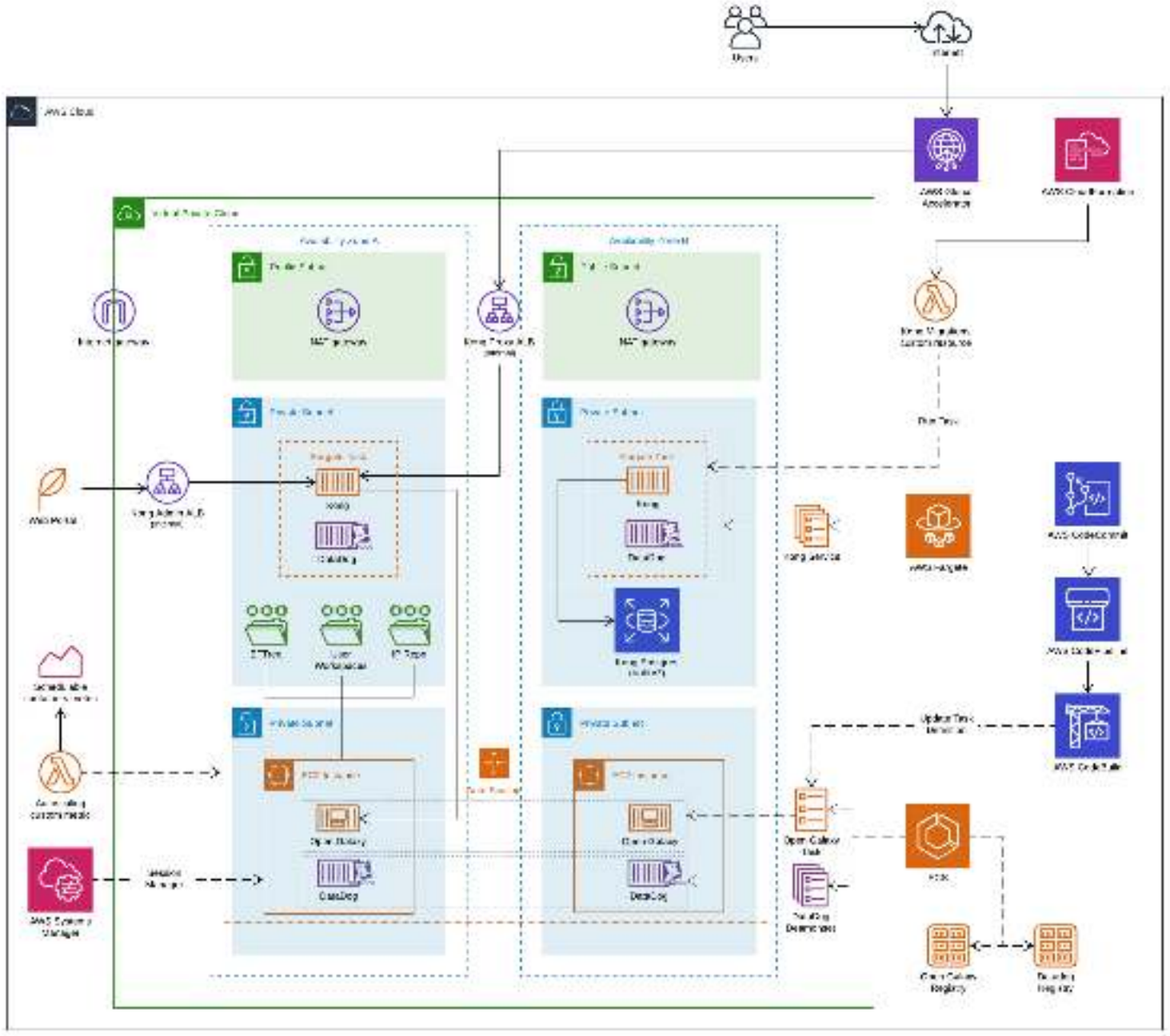
# PROPRIETARY EDA TOOLS

## SIEMENS EDA

- Seamless integration in **efabless** platform
- Complete Mentor/Tanner design flows
- Process technology support 65 through 22FDX
- Optimized SoC template implementation







# CLOUD "WARE"

- Modern
- Secure
- Access control
- Scalable
- Containerized
- AWS (+ awsgov)
- Analytics / traceability



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# KEY PLATFORM FEATURES

- **Instant access** to the platform - **less than 5 minutes**
- **Option for No-NDA** Access To Foundry Process Technology - efabless' obfuscation technology
- **No Upfront Cost** Microelectronics Design Tools (EDA) using proven Open Source & Proprietary SW
- **No IP licensing cost** for prototyping enabled by IP obfuscation
- **No cost Try Before Use/Buy** for proprietary designs while protecting IP information and ownership
- **Low cost prototype manufacturing** options as multi-project-wafers (MPW) including bench setup
- **Built-in project collaboration**, forums and management enabling **effective knowledge exchange**
- Provides **results-based reputation/certification** indicators based on real user design performance
- Supports online **project-based** - design, verification & validation of microelectronics
- **Elastic and scalable** infrastructure to support 10,000's of users
- Marketplace **connecting** designers to potential customers for their **unique design innovation**

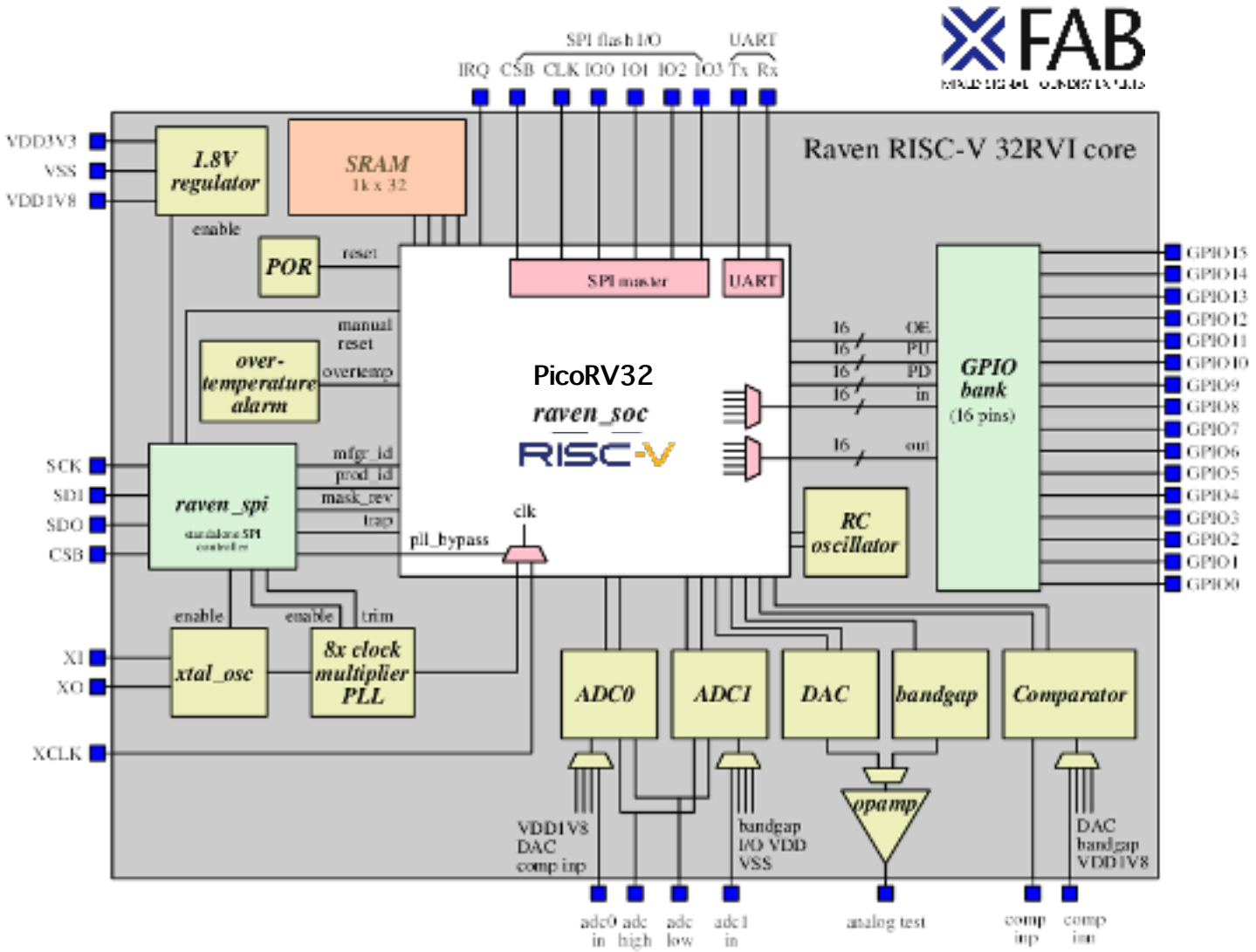
# EFABLESS SoC's

# RAVEN - 32-bit RISC-V uC

## Key Features

- RISC-V CPU (**PicoRV32**)
- SRAM 32x1024
- 100 MHz clock rate
- Programmable clock source
- 16 channels GPIO
- 2 ADCs
- 1 DAC
- 1 Comparator
- Over-temperature alarm
- 100 kHz RC oscillator
- Programmable functions on GPIO outputs
- Programmable interrupts on GPIO inputs

http://github.com/efabless/raven-picorv32



RAVEN

## AES Authentication

- …ntication / Identification / Signature
  - Confirming the user is who or what is stated
  - chip encrypts data with an 'identity key'
  - Key is symmetric

- R-PI have authentication requests verified by the Raven processors externally

| Lines of codes | Max RAM |
|---|---|
| 1.2k | ~128 bytes |



RAVEN

## Audio Sampling and Transfer


1. Data is recorded at 8 …
2. Turn data into digital stream
3. Split to 3 MPC 'random' shares
4. Sent to 3 different servers on cloud

| A/D: #bits | Sampling per second |
|---|---|
| 8 | 8Khz |



## Open Source Based Privacy Preserving Computing for IOT

NEC Corporation
Israeli Research Labs

NEC

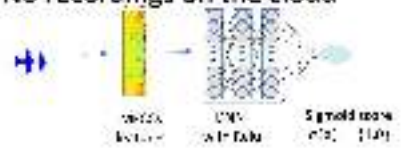
efabless

**For more information about Raven & Ravenna**
**https://efabless.com/design_catalog**

RAVEN

## …udio Sampling and Transfer

…vate voice detection
Private keywork recognition
- Keyword is located in the recording
- No recordings on the cloud



- sMPC random shares are just random numbers

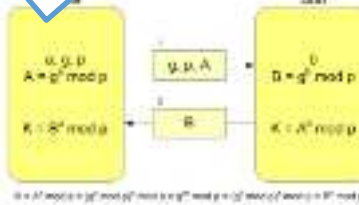
| Lines of codes | Max RAM |
|---|---|
| ~100 | <100 Bytes |



RAVENNA

## PKI Implementati…

- Demo:
  - Standard key exchange Diffie–Hel…
  - Compute public and private keys
  - Ravenna chips



- Best performance
  - Ravenna : 96 bits, 75 seconds
  - Newer Ravenna: 128 bits, 60 seconds

| Lines of codes | Max RAM |
|---|---|
| ~400 | <100 Bytes |

# RAVENNA - 32-bit RISC-V uC

**Features:**

The SoC design incorporates on-board analog functions, including the following:

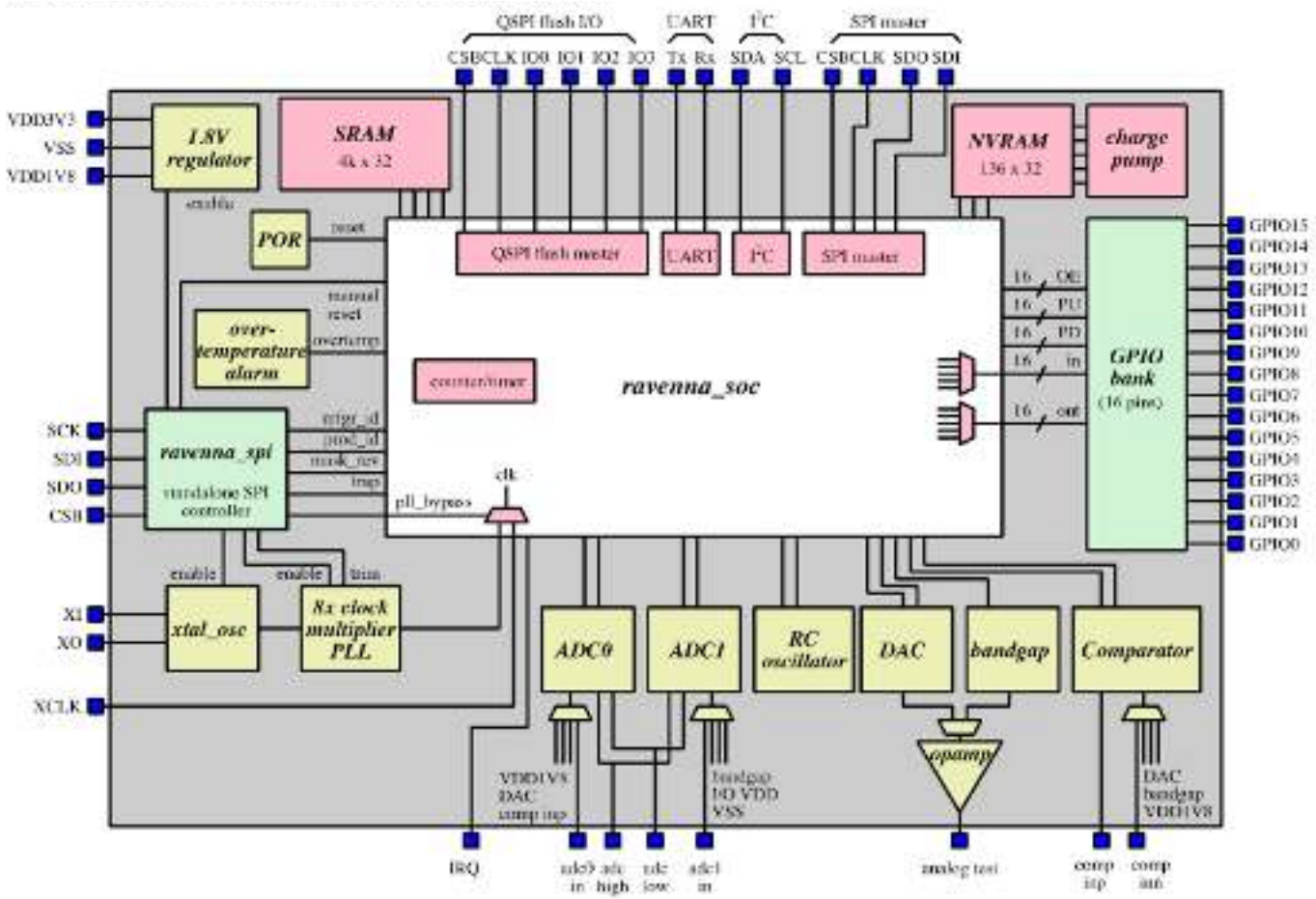
2 10-bit SAR ADCs
1 10-bit DAC
1 analog comparator
1 100kHz RC oscillator
1 1.235V band gap reference 1 high temperature alarm

Digital functions/features of the SoC include:

1 QSPI flash controller 1 UART
1 SPI master
1 $I^2C$ master

1 counter-timer

16 general-purpose digital input/output channels
4k word (4096 bytes × 32 bits) on–board SRAM
136 (128) word (128 bytes × 32 bits) on–board NVRAM




Ravenna PicoRV32 SoC die (2.573mm × 2.068mm)



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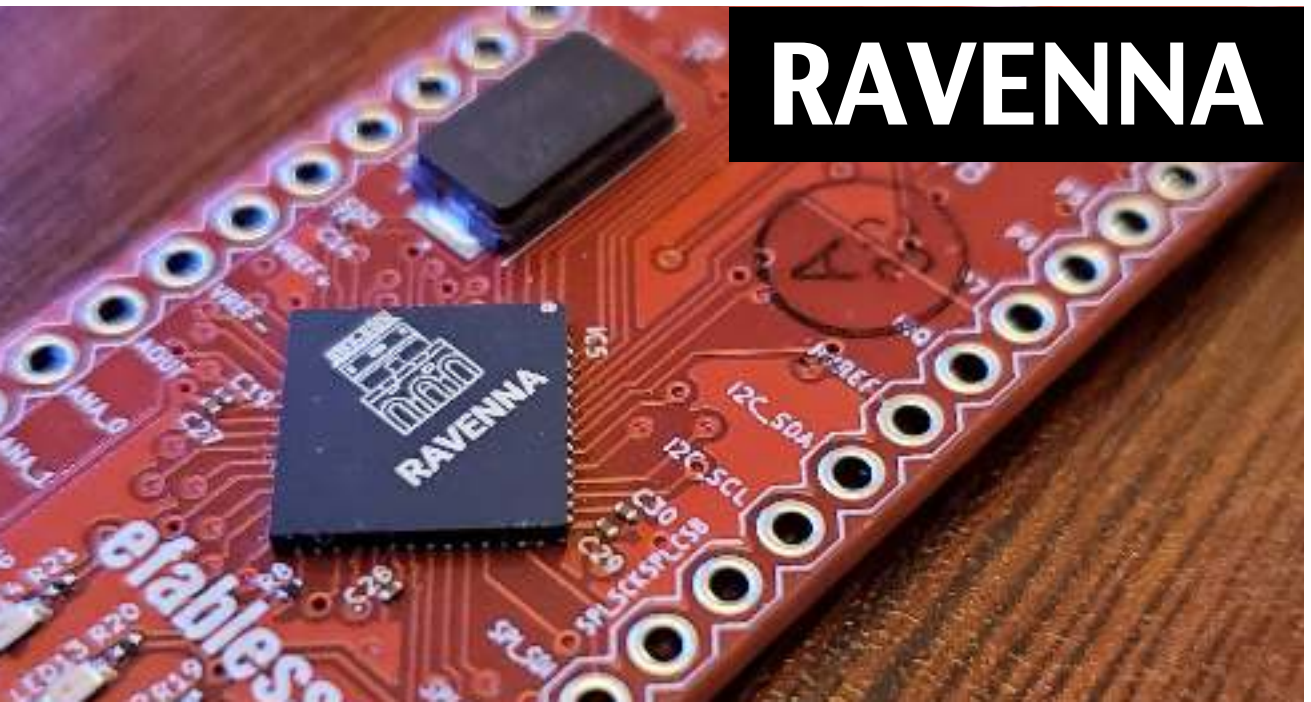
RAPTOR




RAVENNA


HYDRA

# PARTNERS AND CUSTOMERS

## Customers

arm

centauri

dialog SEMICONDUCTOR

Google

LINEAR MICRO SYSTEMS

NEC Orchestrating a brighter world

X FAB MIXED-SIGNAL FOUNDRY EXPERTS

zGlue

## Ecosystem Partners

imec

GLOBAL FOUNDRIES

Si SILICON CATALYST

X FAB MIXED-SIGNAL FOUNDRY EXPERTS

SANKALP semiconductor

antmicro

SyMMiD



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# Open Silicon Prototyping Program

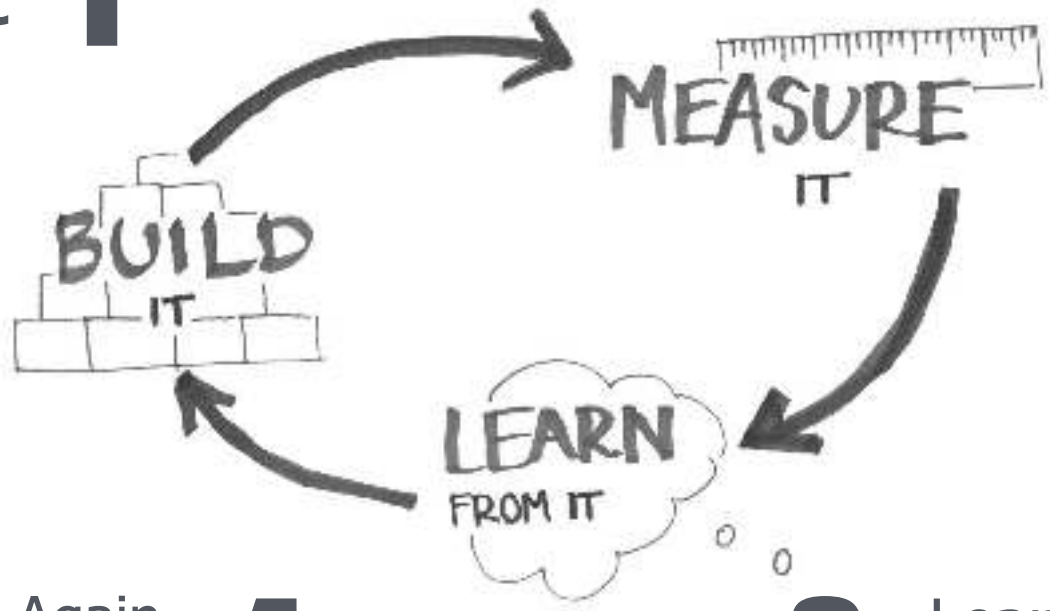


# CONTINUOUS INTEGRATION OF IC'S (CIIC)

**1** Design it

Quick
Cheap

**2** Test It




**3** Learn from it, What works, What doesn't viability, feasibility

**4** Do it Again

Correct & Refine

**Open Source PDK**

**6 open SKY130 runs**



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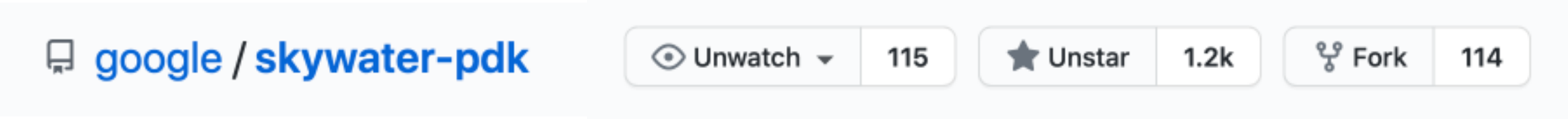
# SkyWater-PDK Released

**June 30, 2020**

github.com/google/skywater-pdk

No NDA, nothing to sign^, just clone and run: *make timing*




**The more we all support it the more it happens**

# Well ....

# What can I do with the 130nm process?

# Intel Chips

13

## 2000
## Intel® Pentium® 4 processor

Initial clock speed:
1.5GHz

Transistors:
42 million

Manufacturing technology:
0.18 micron

14

## 2001
## Intel® Xeon® processor

Initial clock speed:
1.7GHz

Transistors:
42 million

Manufacturing technology:
0.18 micron

15

## 2003
## Intel® Pentium® M processor

Initial clock speed:
1.7GHz

Transistors:
55 million

Manufacturing technology:
90nm

16

## 2006
## Intel® Core™2 Duo processor

Initial clock speed::
2.66GHz

Transistors:
291 million

Manufacturing technology:
65nm

410 million

Manufacturing technology:
45nm

47 million

Manufacturing technology:
45nm

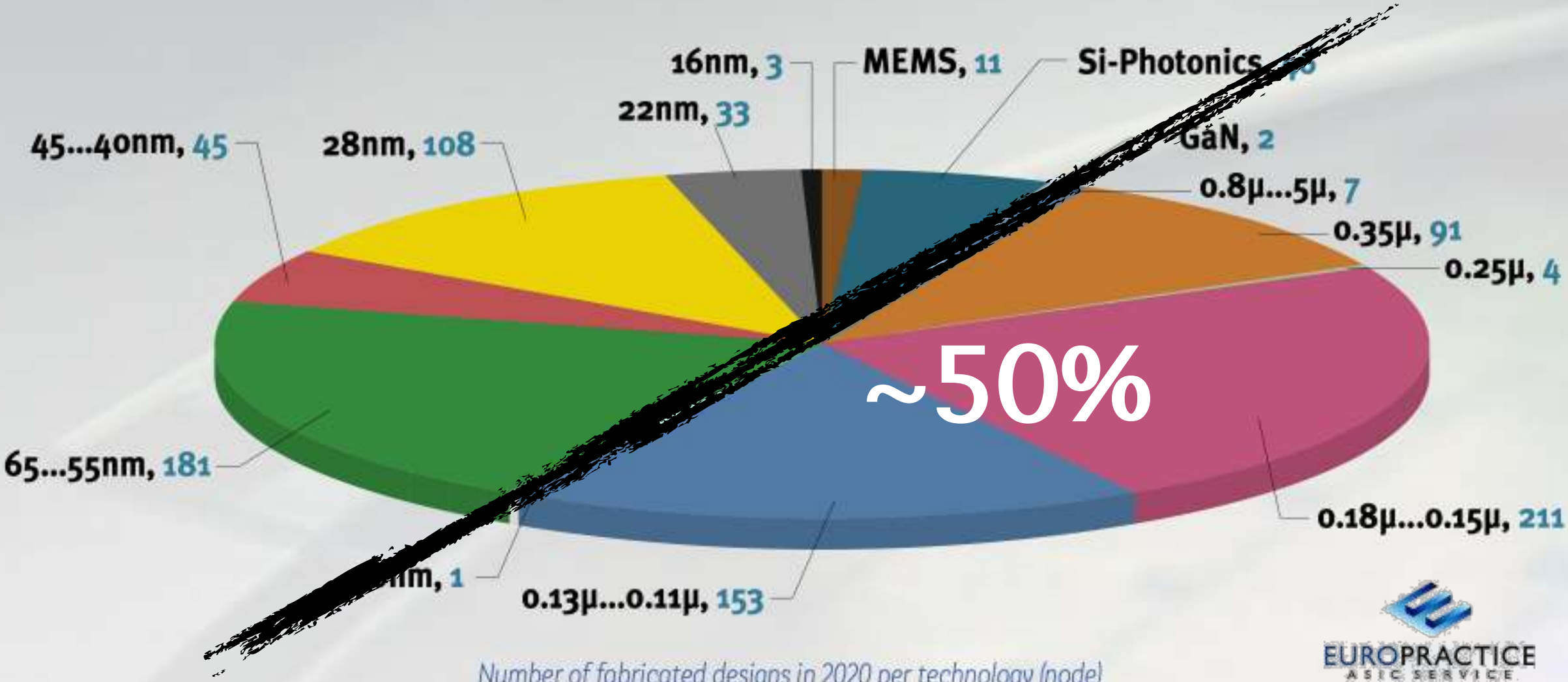
1.16 billion

Manufacturing technology:
32nm

1.4 billion

Manufacturing technology:
22nm

# WE SHOULD WORK ON ALL PROCESSES




Number of fabricated designs in 2020 per technology (node)

EUROPRACTICE
ASIC SERVICE

# FOSSI DIALUP SERIES

FOSSi Foundation

## youtube.com/c/FOSSiFoundation/videos


j.mp/du20-pdk


j.mp/du20-openlane


j.mp/du20-strive


j.mp/du20-stdcells


j.mp/du20-openram


j.mp/du20-magic



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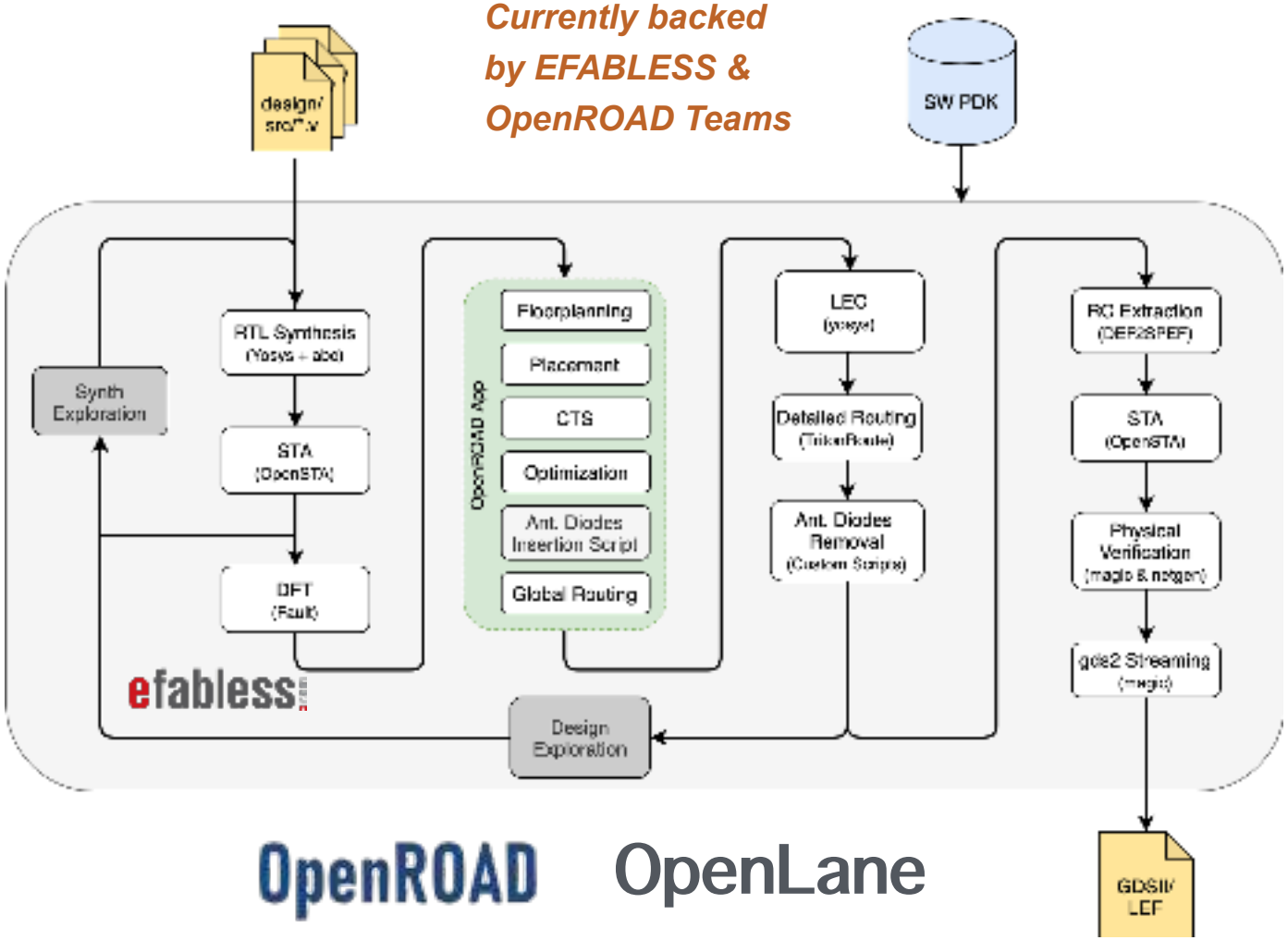
# COMPILER-LIKE RTL2GDS

OpenLane is a no-human in the loop RTL to GDS compiler built around OpenROAD that works like a ***GNU software compiler with trade-offs in area and performance.***

It opens the door for software developers to generate hardware representation without the need for details. **That's at least a 1000X more potential designers!**

***Currently backed by EFABLESS & OpenROAD Teams***




OpenROAD OpenLane

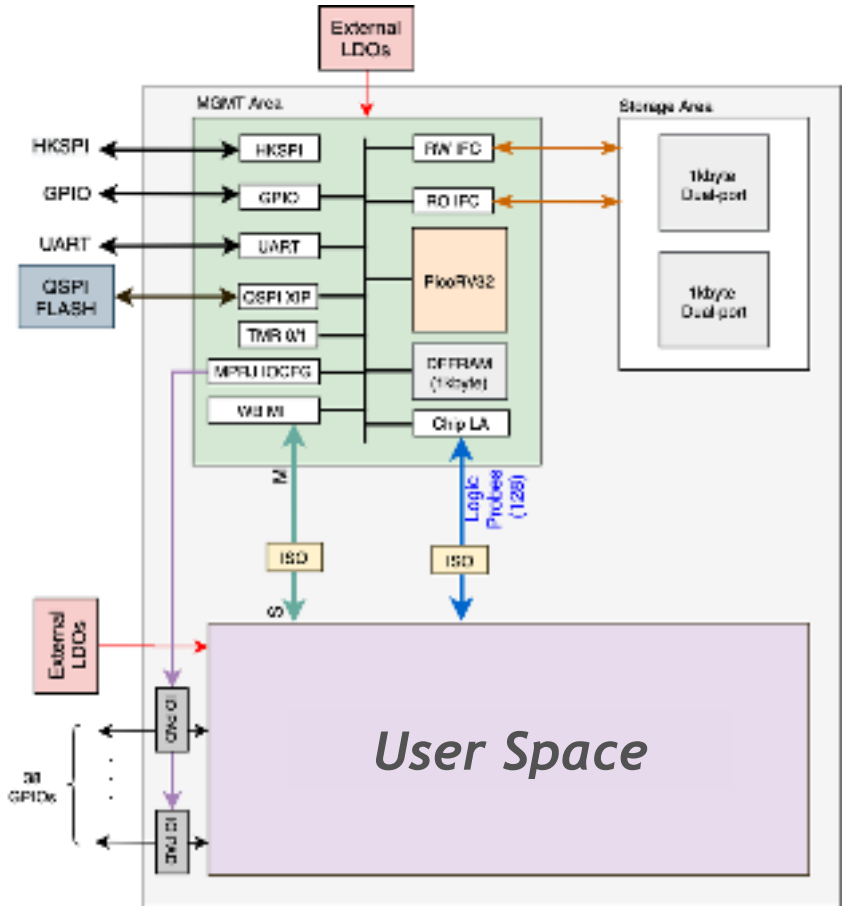
*Supports SKY130, GF130, XFAB180*

*12nm support is under development by OpenROAD team*

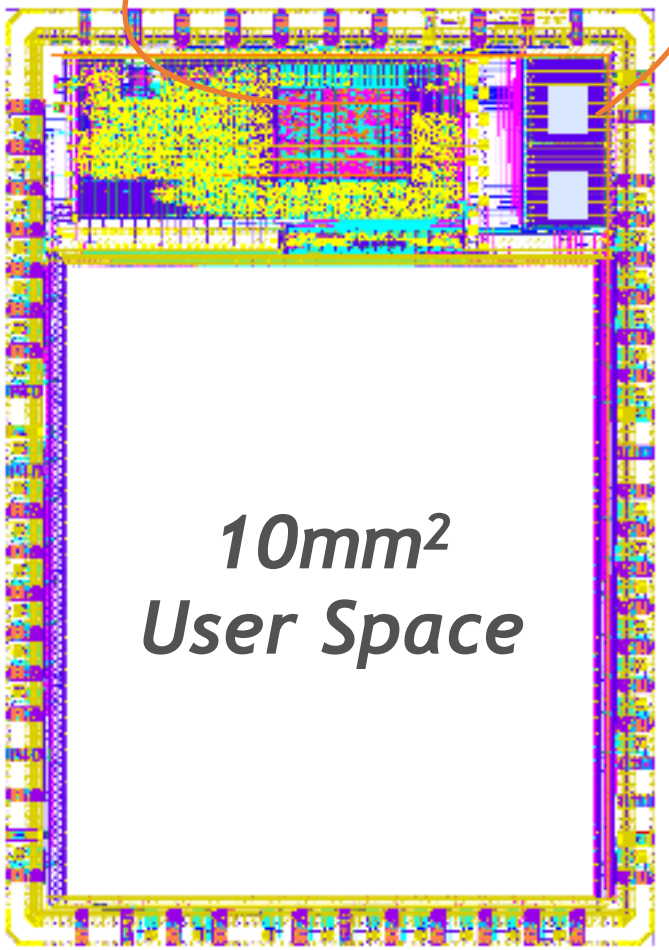


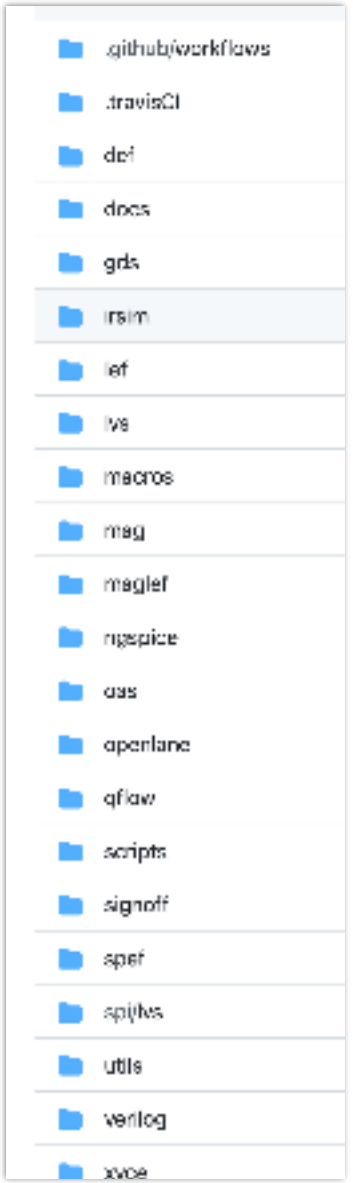
efabless

# CARAVEL HARNESS




PicoRV32 OpenRAM
OpenROAD OpenLane




Uniform Open Source File Structure to ease reuse & modifications

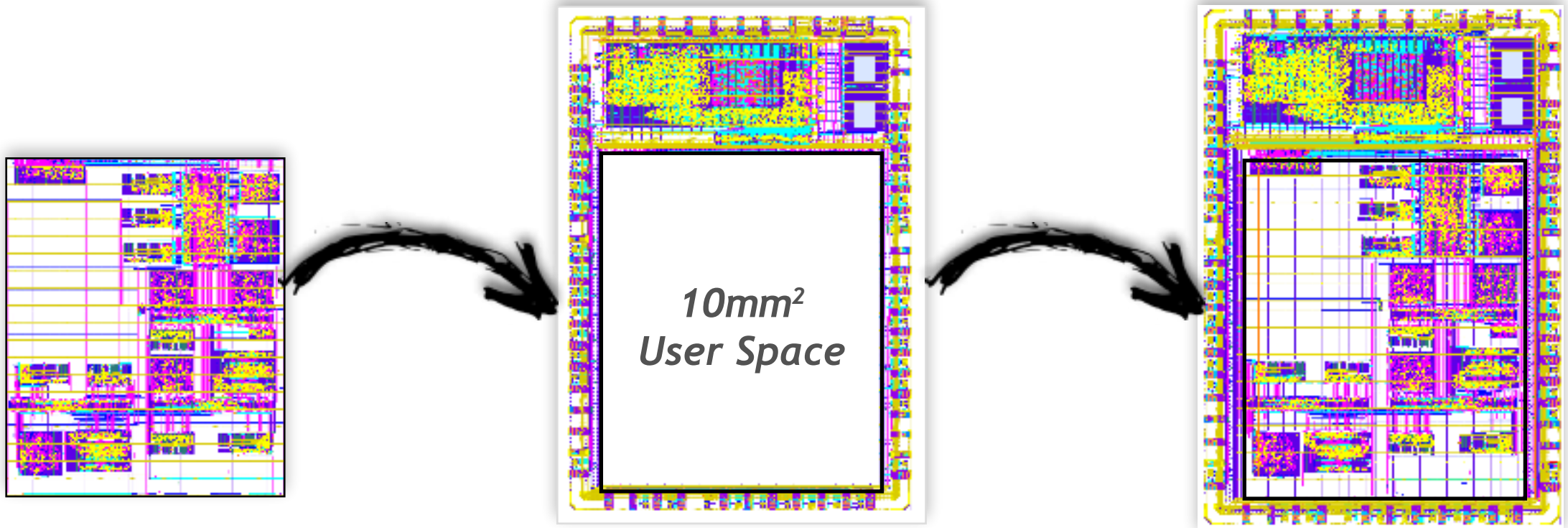
https://github.com/efabless/caravel

CARAVEL Platform



efabless.com

# CARAVEL HARNESS - HOW IT'S USED




USER DESIGN

CARAVEL

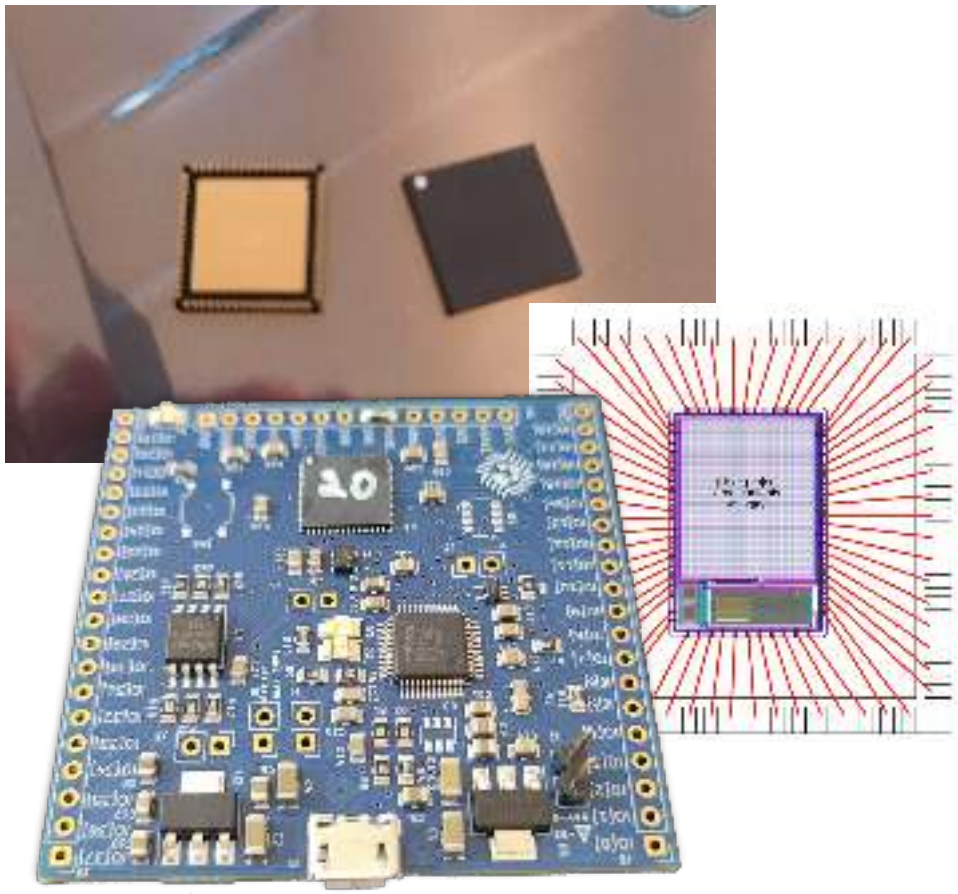
CARAVEL

https://github.com/efabless/caravel



efabless.com

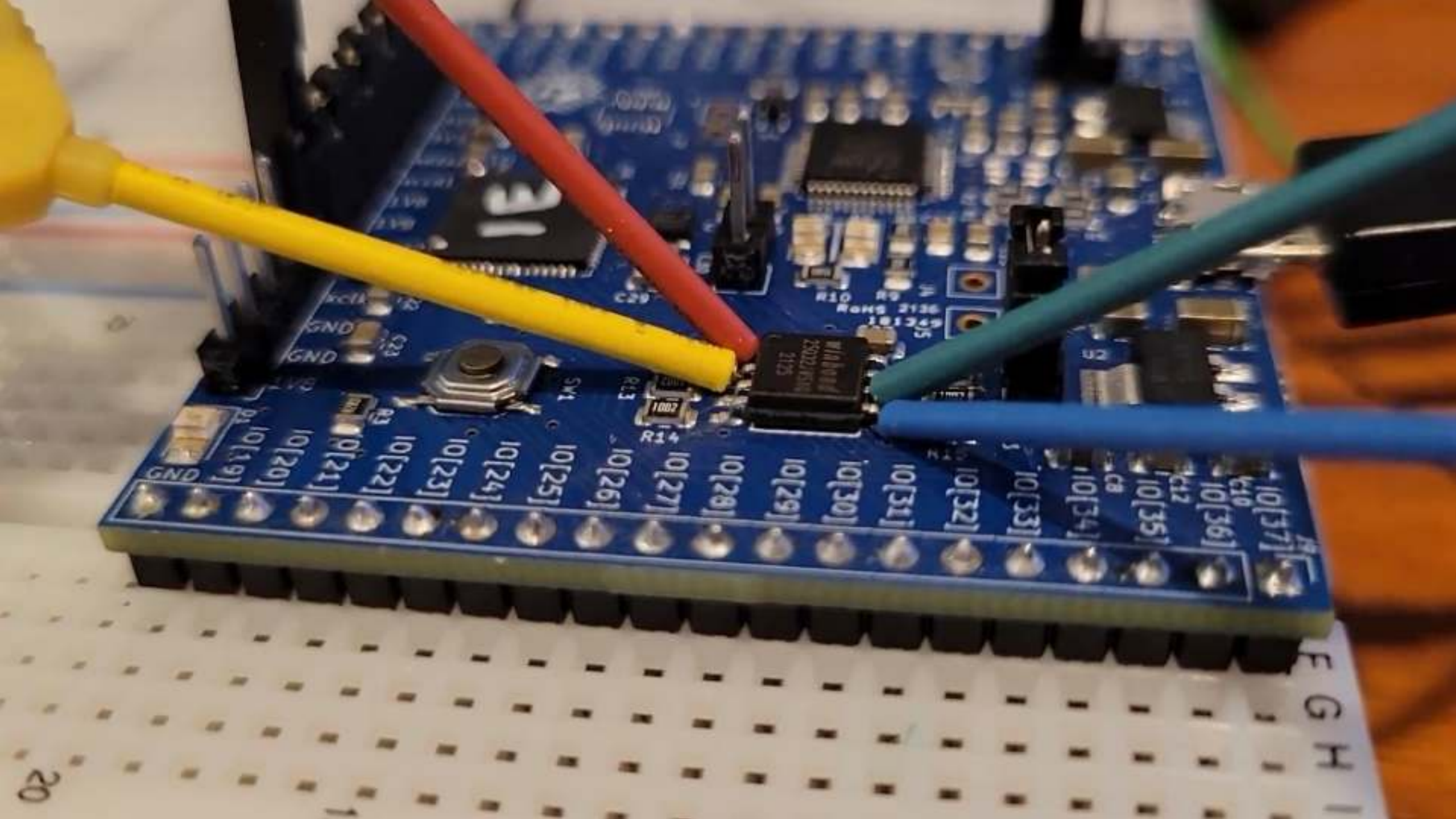
# SILICON VALIDATION



*Actual Chip and Board Images*

- Users receive **packaged chips** as well as **assembled 5 evaluation boards** with their projects

- An open-source software test framework is available for the program including
  - Logic Analyzer
  - Drivers for common peripherals
  - Flash programming utility
  - Example firmware routine for common functions
  - Instructions for extending the test examples for your project


GND
GND
GND
C29
R10
R9
SW1
R13
R14
C23
C8
C12
C10
IO[19]
IO[20]
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IO[37]
20

# ENGAGEMENT IN NUMBERS - SLACK SPACE

**2,000+**

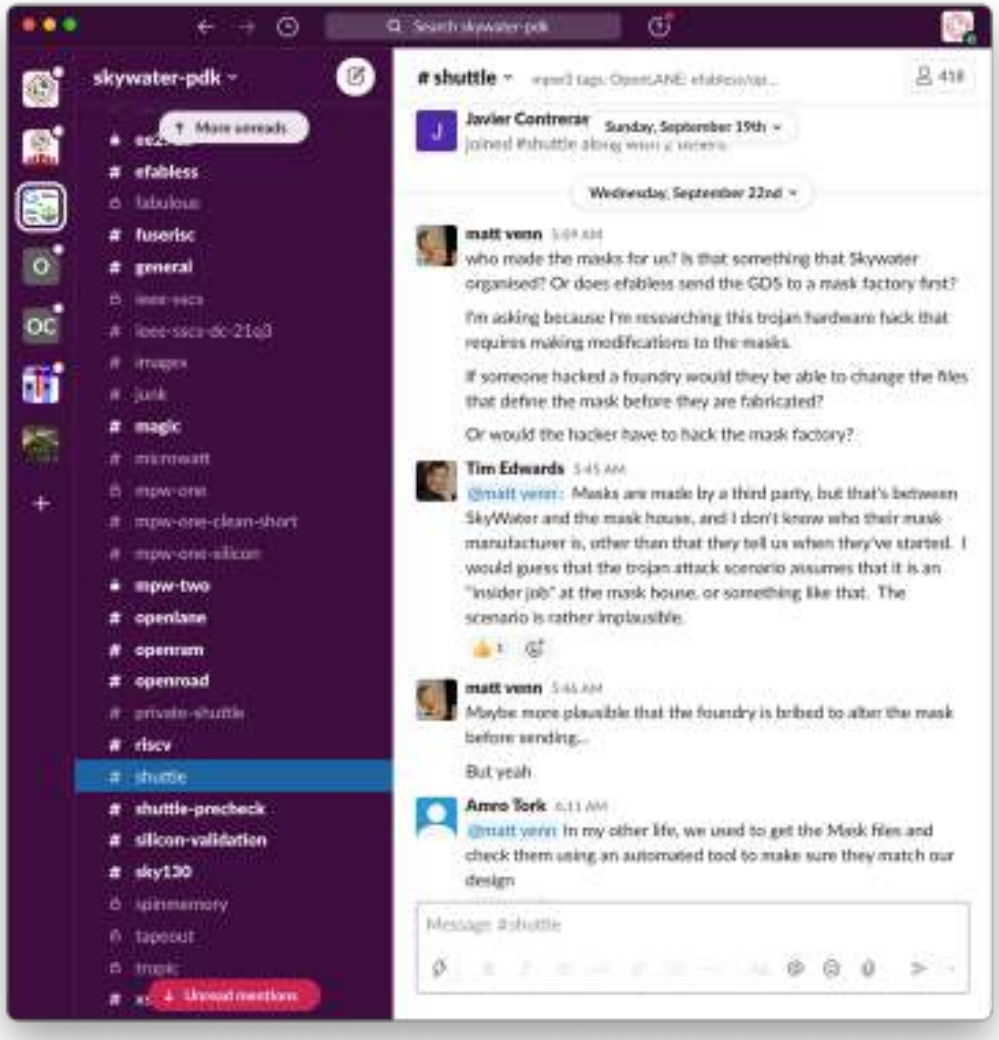
COMMUNITY MEMBERS

**100+**

CHANNELS & TOPICS

Join SkyWater-PDK Community

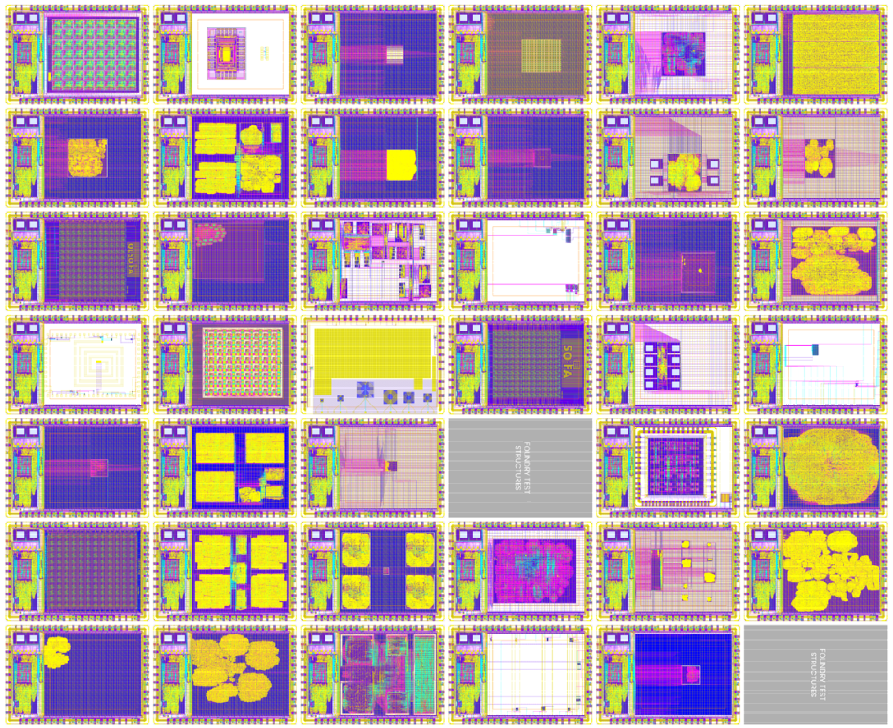
https://join.skywater.tools






efabless.com

# The first shuttle was overbooked: 45 designs submitted in 30 days!

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Sponsored by Google

## DESIGN TYPES - MPW ONE

- 9 x Open processor cores
- 9 x SoC's
- Crypto-currency Miner
- Robotic App Processor
- Amateur Satellite Radio Transceiver
- 7 x Analog/RF
- 5 eFPGA's

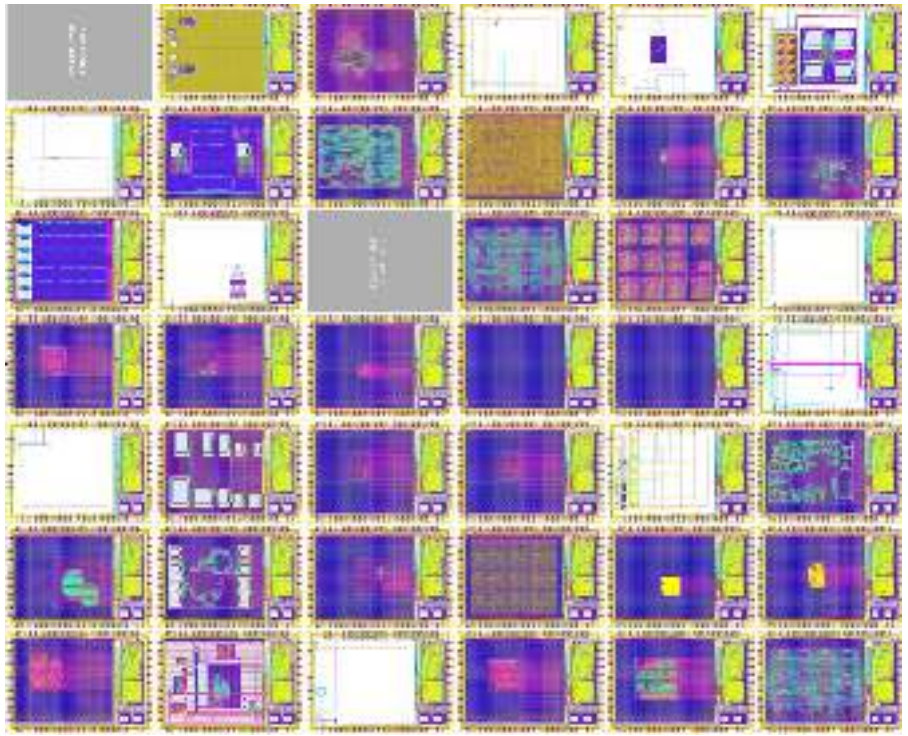
***All designs must be Open Source***



See Projects Here: https://efabless.com/projects/shuttle_name/MPW-1

efabless.com

# And so was the second: 56 designs submitted in 30 days!



# Open MPW Shuttle Program

efabless.com

Sponsored by Google

## DESIGN TYPES - MPW TWO

- 11 x Open processor cores
- 11 x SoC's
- Crypto-router
- Time to Digital Converter - LIDAR
- Multi-project harness for Caravel x 16
- 17 x Analog/RF
- 2 eFPGA's

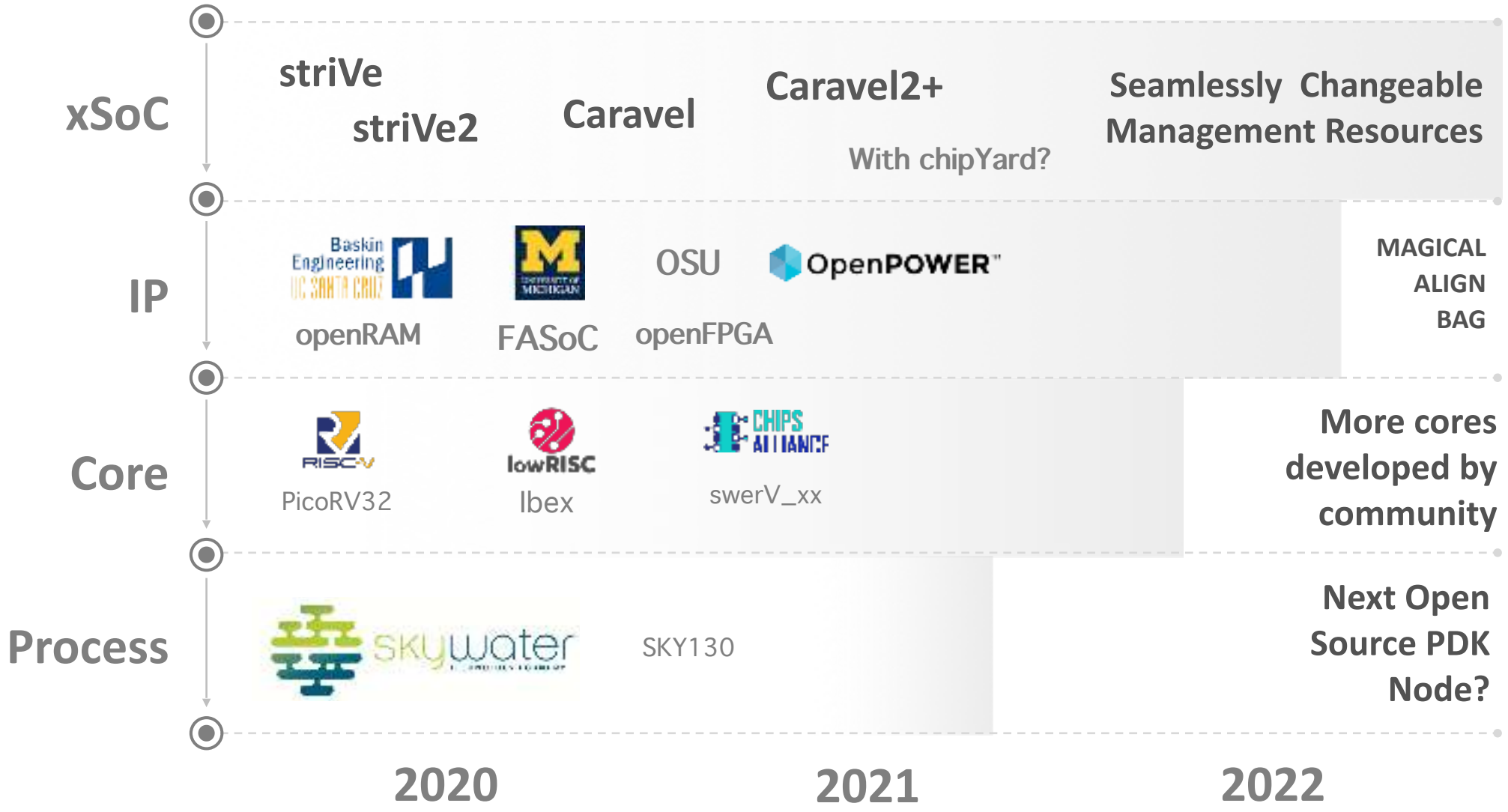
***All designs must be Open Source***



See Projects Here: https://efabless.com/projects/shuttle_name/MPW-2

efabless.com

# KEEP MOVING - MORE IS COMING






efabless.com

# BUT ....

What if do not want to open source my design?

I would like to book & guarantee my spot!

I seriously care about the schedule.

chipIgnite


## Includes:

- Complete EDA design flow
- Automated physical implementation for digital designs
- 37 programmable IOs supporting digital and analog
- Pre-designed packaging and evaluation board
- Supports commercial EDA options as well
- QFN or WCSP packaged parts based on shuttle
- 10 mm² user design area
- 5 evaluation board assemblies
- 100, 300 or 1000 packaged parts

## Schedule:

| Shuttle | Tapeout | Delivery | Parts |
|---|---|---|---|
| MPW-Q2106 | June 18, 2021 | October 6, 2021 | 100 QFN |
| MPW-C2110 | October 15, 2021 | January 31, 2022 | 300 or 1000 WCSP |

**Note:** Schedule depends on meeting minimum project capacity
$200 reservation fee (fully refundable if minimum projects not met)

## 1 Evolve your Design Idea

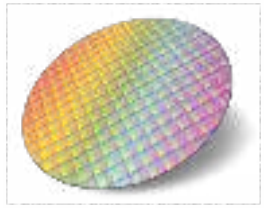
- Explore/what-if/trade-offs
- Simulate, verify, iterate
- Design, verify, modify layout
- Collaborate, brainstorm with others

## 2 Design-Ship ToolBox

- Carrier SoC Harness
- Predesigned ESD Protection
- WCSP Packaged
- Starter IP design library

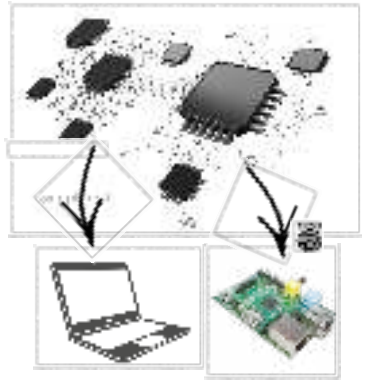
## 3 Send to Manufacturing

- Multiple foundry partners
- Multiple process options
- Unprecedented die area cost/mm
- Get samples + dev boards by mail



## 4 Validate your Design

- Get a well-equipped tester board
- 16 Analog/32 Digital Channels
- Standard Test description language
- Laptop or Raspberry Pi driven
- Correlate with pre-silicon sims




# chipIgnite

1) **No open source requirement**
2) **Guaranteed space on shuttles**

Large and rapidly growing demand in US and overseas

Initial focus on education and research

efabless.com

# chipIgnite

**customers since June 2021**

**1** Stanford EE272 Design course

*Three additional universities & one startup running projects*

**Pipeline is building**

IEEE SOLID-STATE CIRCUITS SOCIETY™ IC Innovation

**2**

SSCS "**PICO**" Open Source Design Contest:

**56+** **submitted designs**

**10** **will tape out at Efabless**


Open Source FPGA Foundation global program innovation among university students

**3**

**2** ChipIgnite Slots per University

Turkey, Pakistan, India, Australia

efabless.com

# chipIgnite

## FOR UNIVERSITIES

Undergraduate courses

Capstone projects

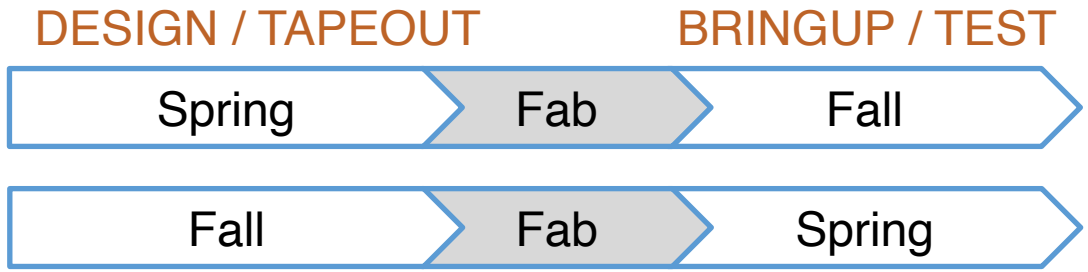
Graduate Research

skywater

efabless.com

# TAPE-OUT COURSES

- Analog and / or Digital Design Courses
- Two-session courses:




- Single session courses:
  - Design + test via FPGA
  - Design + test previous student project
  - Test broken design + fix and tapeout
  - Future: one course period design/tape-out/test



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# EFABLESS FOR WORKFORCE DEVELOPMENT

efabless all-in-one platform makes it possible to engage 1000's of students at any stage of education in real life learning experience in design, verification, prototyping and validation of microelectronics

# WORKFORCE DEVELOPMENT AT A GLANCE

| Audience | Goal | Complexity | Cost | Scale | Commercial Applicability | Requirements |
|---|---|---|---|---|---|---|
| **High School** | More Interest | LOW | LOW | 100,000's | LOW | Mature nodes, open-source |
| **Undergraduate** | Expertise | MEDIUM | MEDIUM | 10,000's | SELECTED | Mid-nodes, open-source + commercial |
| **Graduates** | Adv. Expertise Novel IP | HIGH | HIGH | 1000's | HIGH | Advanced nodes, commercial tools |

# CALL TO - ACTION

## It is a massive undertaking we should work together

## Repeat good examples

Apple awarded innovation grants to engineering schools at four **historically black colleges and universities to** expand their coursework, scholarships, and internship opportunities in hardware engineering and silicon chip design.

# Thank you!

# Get Involved - Useful Links / Repos

## Information Hub

github.com/efabless/skywater-pdk-central

- Join SkyWater PDK Slack Space - https://join.skywater.tools
- The OpenLane flow for digital PnR can be found at https://openlane.io
- The OpenROAD Project https://theopenroadproject.org/
- The documentation is at https://docs.skywater.tools
- MPW-ONE https://efabless.com/open_mpw_shuttle_project_mpw_one
- Caravel documentation https://caravel-harness.readthedocs.io/en/develop/index.html
- WOSET/ICCAD Workshop on EDA https://woset-workshop.github.io/WOSET2020.html