CHIPS Alliance

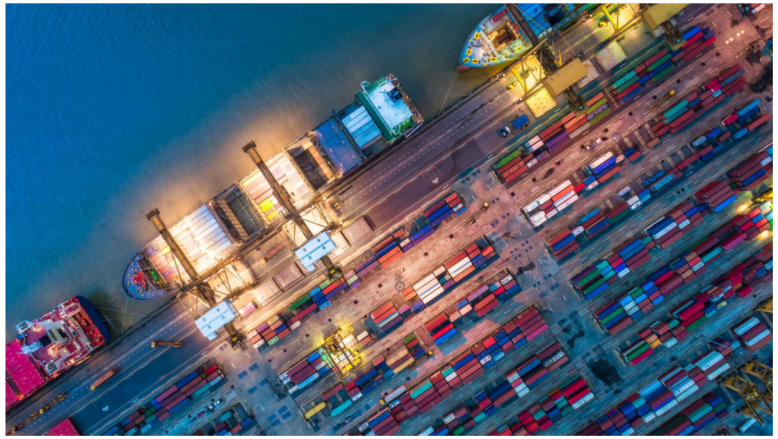
Rob Mains
General Manager
CHIPS Alliance

Email: rmains@linuxfoundation.org
Phone: +1 408 607 4879

CHIPS ALLIANCE

Industrial Evolution: Siloed to Collaboration

Soup to Nuts Silo: In House

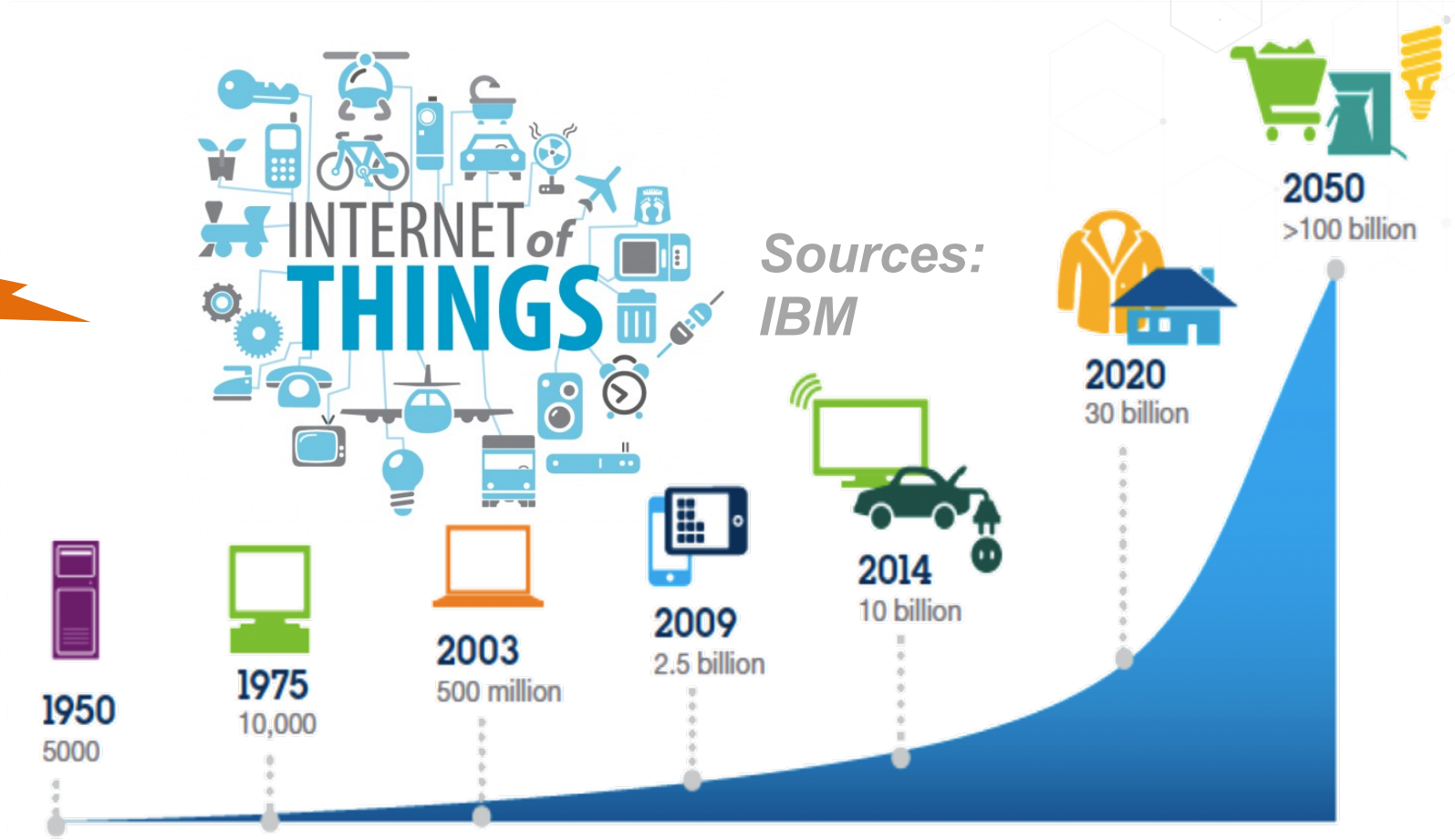


Supply Chain Management: Just in Time delivery

Open Collaboration

CHIPS ALLIANCE

What going on in Hardware?



CHIPS ALLIANCE

CHIPS Alliance: Part of the Linux Foundation

- **1500+** Members From 40+ Countries
- **100%** of Fortune 100 Tech & Telecom
- **30000+** Developers Contributing Code
- **200+** Open Source Projects
- **$16B+** Shared Value

CHIPS ALLIANCE

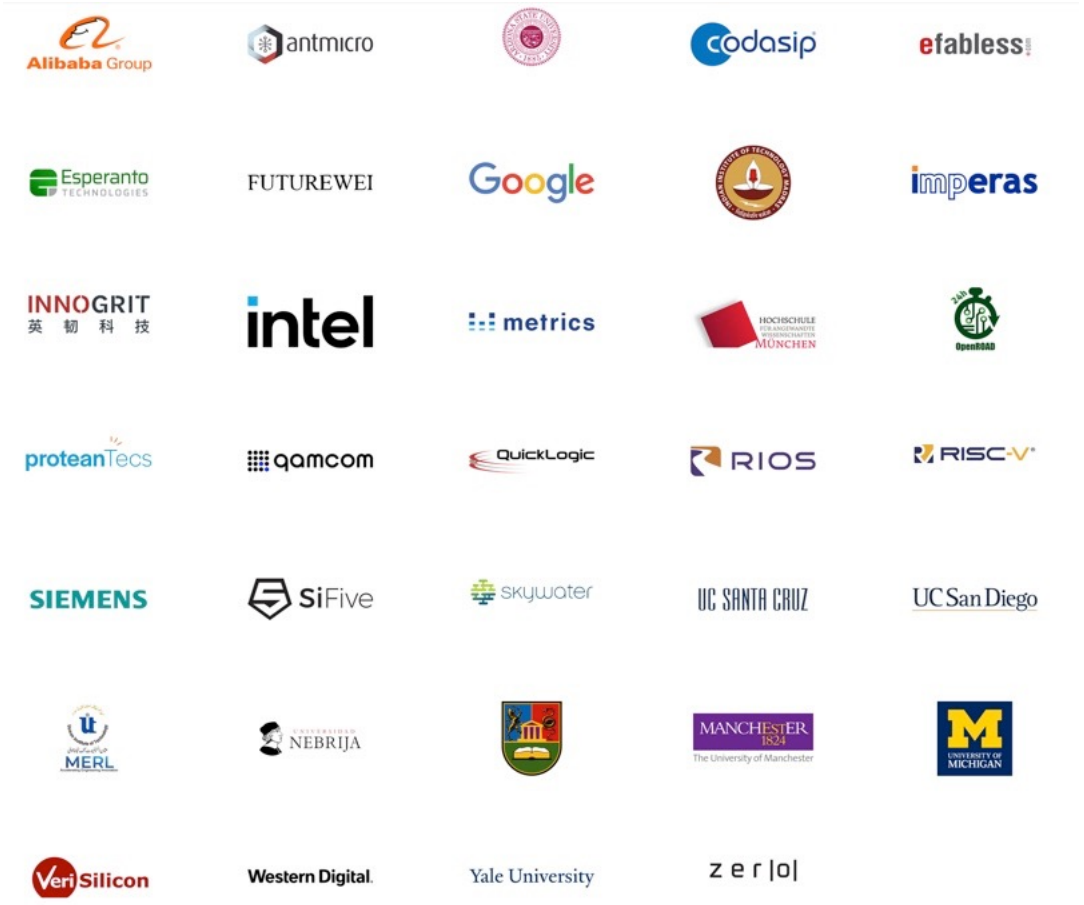
Security	Let's Encrypt, CORE INFRASTRUCTURE INITIATIVE
Networking	LF NETWORKING, ONAP, OPEN DAYLIGHT
Cloud	kubernetes, CLOUD FOUNDRY, CLOUD NATIVE COMPUTING FOUNDATION
Automotive	AUTOMOTIVE GRADE LINUX
Blockchain	HYPERLEDGER
Edge/IoT	LF EDGE, yocto PROJECT, Zephyr™
Web	node.js, JS Foundation, GraphQL
AI	LF AI
Motion Pictures	ASWF /* ACADEMY SOFTWARE FOUNDATION

What is CHIPS Alliance?

- Organization which develops and hosts:
  - Open source hardware specification, implementation, verification
    - Interconnect IP (physical and logical protocols)
      - CPUs
      - I/O (memory, SERDES, network…)
      - ML Accelerators
  - Open source ASIC & FPGA development tools
    - Design, verification, simulation
    - Composition, electrical verification
  - A barrier free environment for collaboration
    - Standards organization for collaboration and development
    - Legal Framework: Apache v2 license
    - IP contribution encouraged but not required for membership/participation
  - Shared resources ($ and time) which lower cost of hardware development

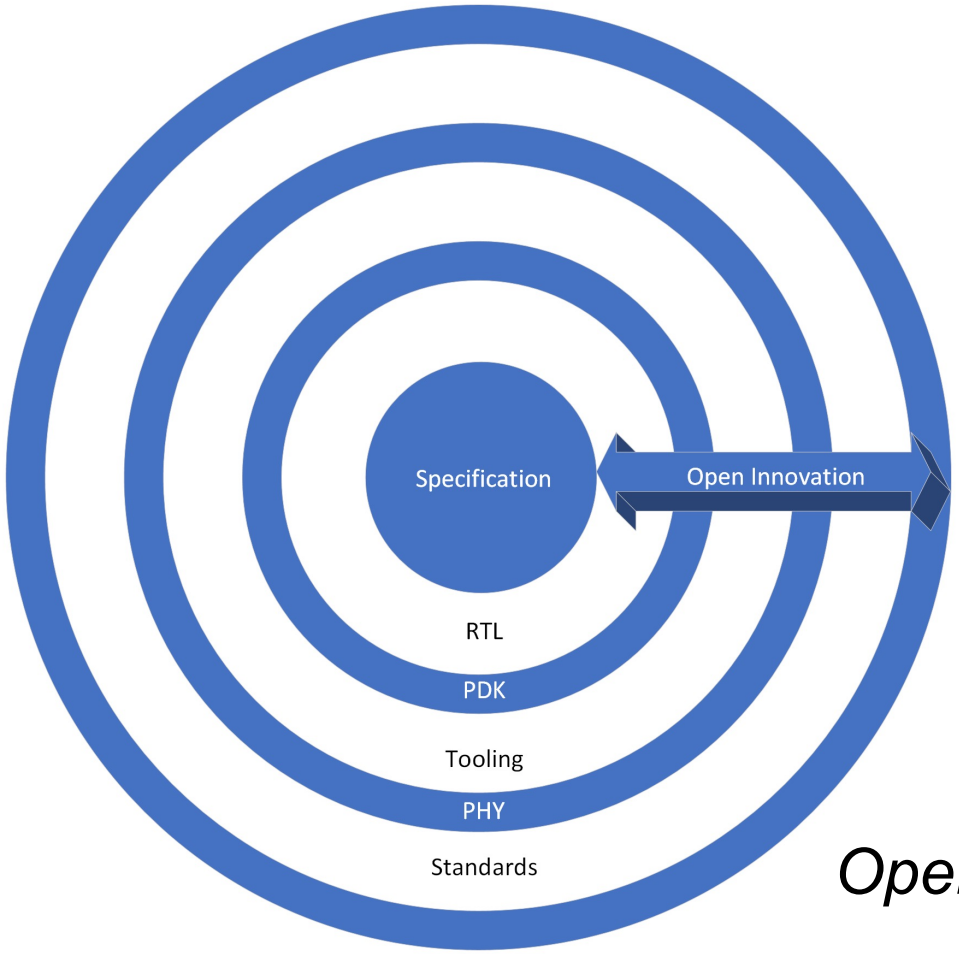
CHIPS ALLIANCE

CHIPS Alliance Members: 38 members and Growing



CHIPS ALLIANCE

Concentric Collaborative Innovation: Open Design Ecosystem



Many Participants

- Individuals
- Universities
- Foundations
- Industry

Opening Pandora's Box: No mysteries

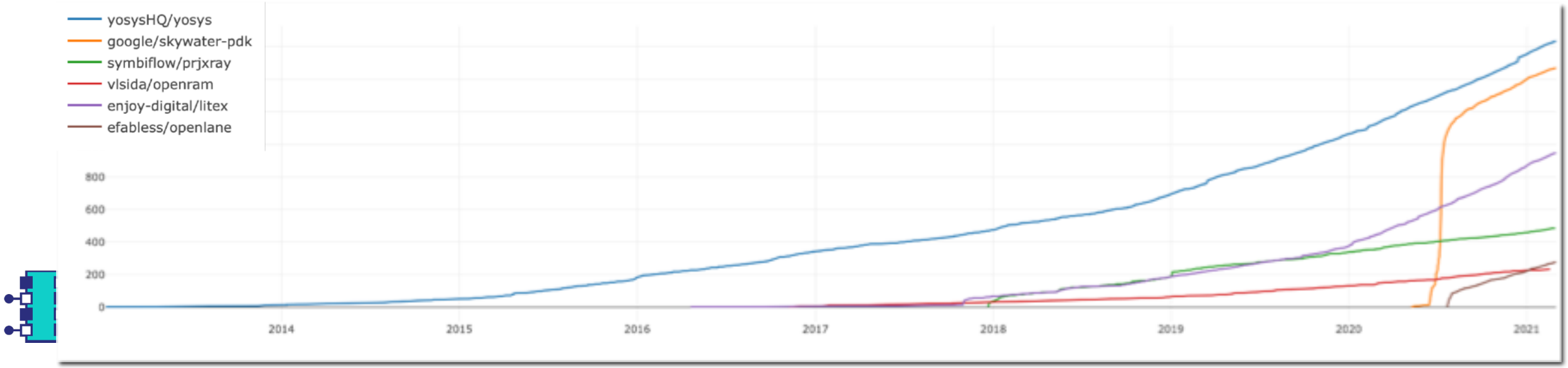
CHIPS ALLIANCE

Open Source PDK's

Skywater-PDK Released
June 30, 2020

github.com/google/skywater-pdk

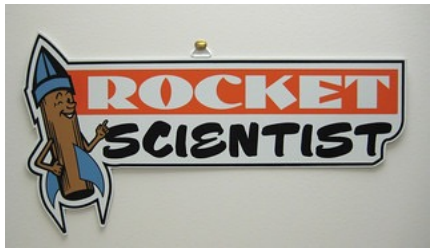
No NDA, nothing to sign^, just clone and run: *make timing*



Mixing Oil & Vinegar: Hardware vs. Software Culture

Hardware

Software

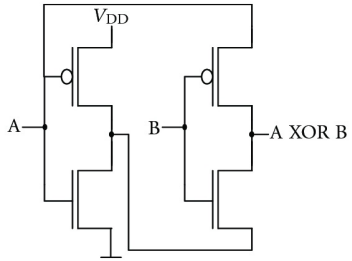


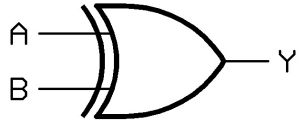
How do we get more people to participate?

CHIPS ALLIANCE

Making Chip Design Approachable

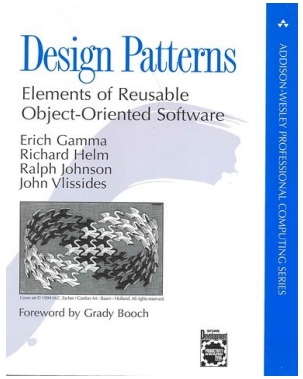
Hiding Complexity -> Increasing Productivity

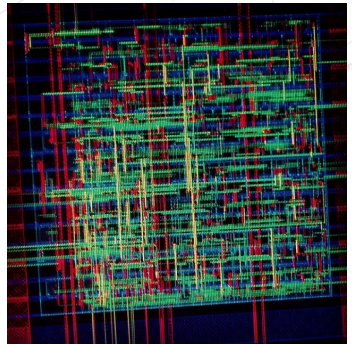





```
// clocked version (not working yet)
always @ (posedge EM_CLK)
begin
    if (!EM_nCE1 && !EM_nWE) begin
        mem[em_addr] <= EM_D;
    end
    if (!EM_nCE1 && !EM_nOE && EM_nWE) begin
        em_outdata <= mem[em_addr];
    end
end

endmodule
```





Transistors

Hand Tuned,
Placed, &
Routed

Gates

First Level
Abstraction

RTL

CHISEL
System Verilog
System C
Verilog
VHDL

Software Concepts

Object Based
Libraries of Services
Ease of Reuse
Integrated Verification

Compilation

Automation Key!
-Layout
-Logic Synthesis
-Place & Route
-Electrical Verif

Increasing Productivity with Less Resource

CHIPS ALLIANCE

But, the devil is in the details. Fundamentals Still Matter!

Challenges with Open Source EDA Software

- Technology access
  - Fundamental information required, frequently requiring an NDA
- Developers
  - Unique mix of hardware and software skills
  - Detailed knowledge of highly specialized areas often required
- Testing, Qualification, and QOR
  - Regression testing and QOR key part of development process
  - Qualification to foundry data key aspect
    - Does it correlate extraction and timing (field solver / spice level)?
      - Test circuits, metal stacks
    - Does it adhere to design rules: DRC correct?
- Methodology & Support
  - Domain experts needed to apply software base to design development
  - Support needed to diagnose problems, resolve issues

CHIPS ALLIANCE


open
hardware
diversity
alliance
Making Open Hardware more diverse, equal, and inclusive!

Thoughts on building an Engineering Community

- Open source environment
  - Allows folks to see the entire picture. No mysteries!
  - Eliminate or reduce silos
  - Help mature the open source hardware & EDA environment
  - Remove legal barriers to collaborative innovation. No NDA's or Umbrella NDA's, not multi-way
- Collaboration between industry, university, secondary schools
  - Engage students early, allow them to see how they fit in the big picture and importance of their contribution
    - *Internships key to allowing students to see why coursework matters*
    - *Tell young engineers how they fit into the big picture*
  - Fund research at universities, but also adapt to your product development
  - Build an emergent, diverse engineering workforce
- Proactive Mentoring
  - Take interest in individual careers and challenges
  - Encourage publication, speaking, leadership

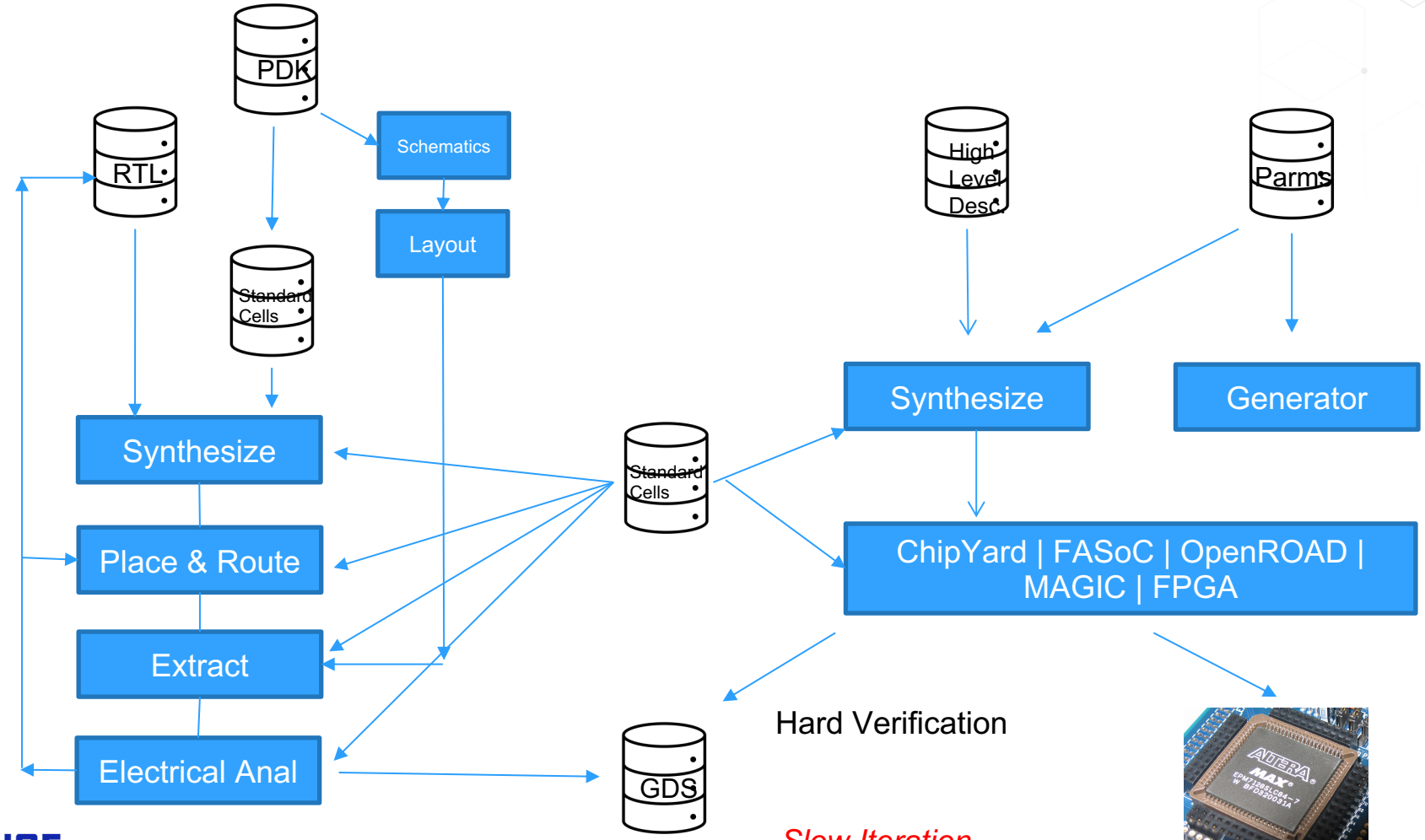
CHIPS Alliance

Rob Mains
General Manager
CHIPS Alliance

Email: rmains@linuxfoundation.org
Phone: +1 408 607 4879

CHIPS ALLIANCE

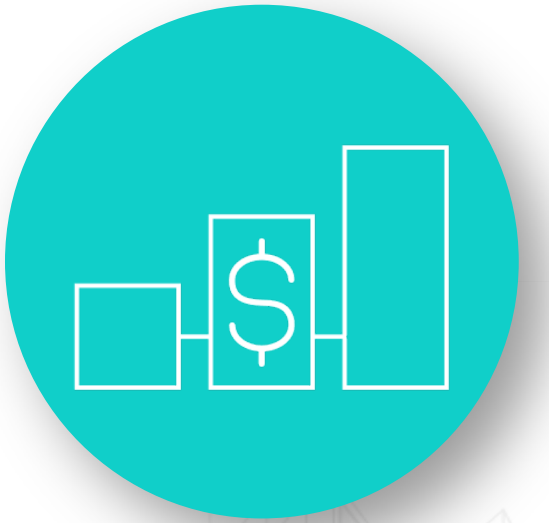
Proving in Design More Quickly: Need for Rapid Iteration



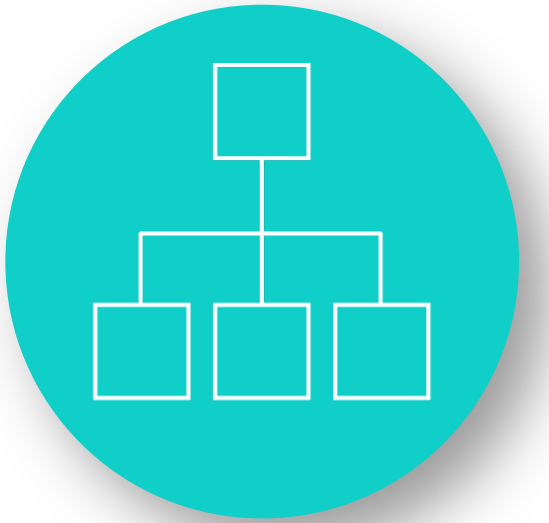
CHIPS ALLIANCE

Traditional Physical Flow

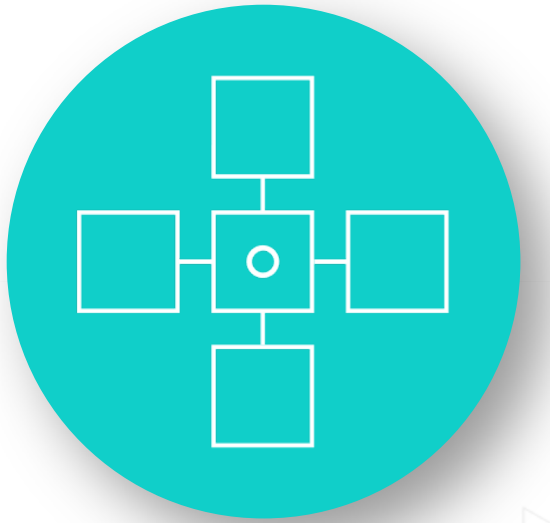
Compute and Design Challenges



Costs of hardware increasing significantly



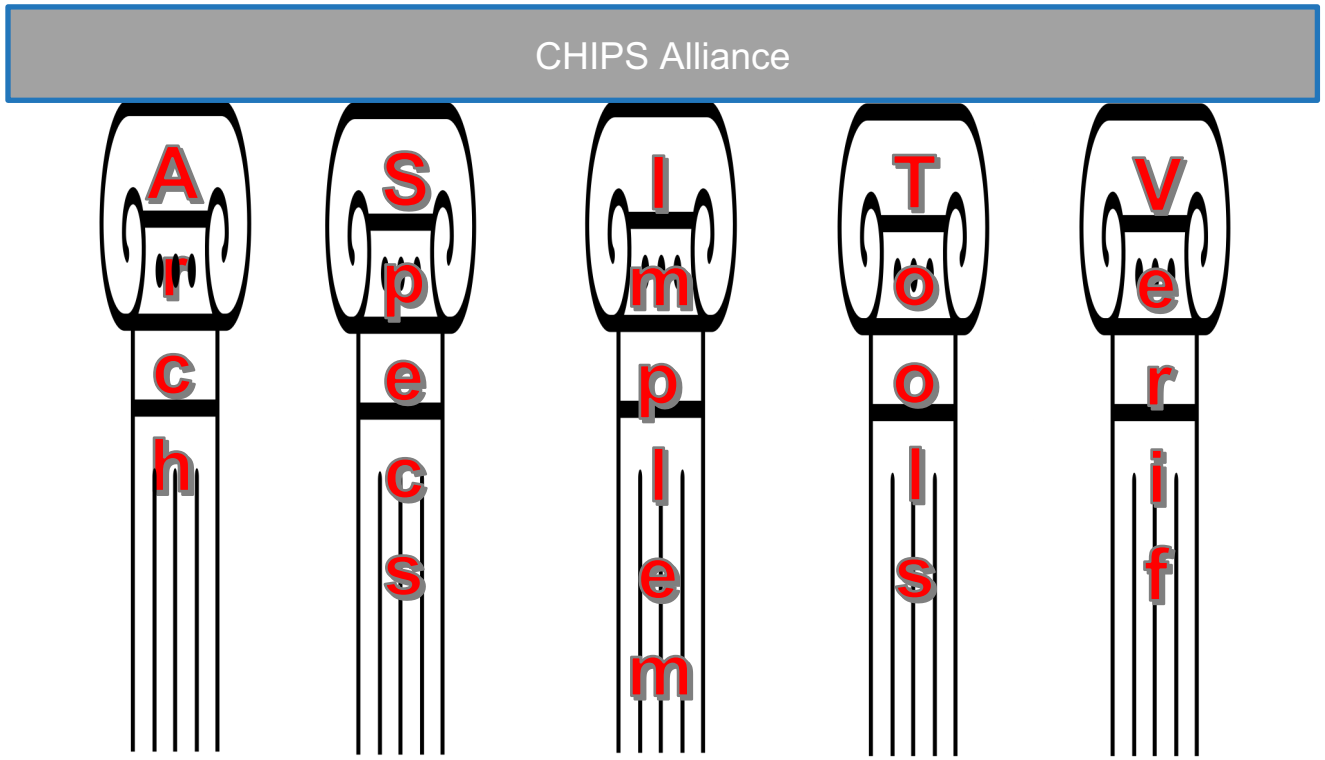
Innovation often stalled in corporate structures



Need more purpose-built architectures

CHIPS ALLIANCE

CHIPS: Pillars of Interest and Opportunities



- Venue for Collaboration
- IP Contribution Welcome, but not required to join
- Level of Participation is up to you!