NSF Integrated Circuits Research, Education, and Workforce Development Workshop

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"Who Am I? Why Am I Here?" Adm. James Stockwell, 1992

- **Who Am I?**
  - **"UCSD"**
    - **Physical design**
    - **Chip implementation (RTL-to-GDS, signoff, PPAC)**
    - **Design for manufacturability**
    - **Technology roadmapping** (ITRS: **design technology**, system drivers)
    - **Open-source EDA** (from the Bookshelf to OpenROAD)
    - **Machine Learning in EDA** and IC design (from METRICS to METRICS2.1)
  - **"OpenROAD"**
    - OpenROAD (2018-22)
    - TILOS NSF AI Institute (partially supported by Intel) (2021-26)
  - **"Startup"**
    - Blaze DFM (2004-07), Cadence (1995-97)

- **Why Am I Here?**
  - *Only Matt knows!*
  - **CAD/EDA advocacy: engine of design productivity, equivalent scaling**
  - **Learn from and be inspired by others**

What are the top 5 CAD research challenges in the next 5 years?

- **Usual litany =**
  - Reliability and error-tolerance
  - Embedded software (e.g., for massively multi-core SOC)
  - Parametric yield and cost optimization
  - Predictable and high-quality IC implementation
  - Beyond-CMOS, 3-D, …
  - Incremental optimizers, successive-approximation optimizers, …

- **Research productivity**
  - Software reuse
  - Research infrastructure
  - Killing problems dead and moving on…

ABK Life Rule #34: "You get what you incent

What are the top 5 CAD research challenges in the next 5 years?

- **People**
  - Is EDA attracting the best and the brightest?
  - Are we here for job security or to solve problems?
- **Culture**
  - Research and technology agendas “made in our own image”
  - Pulling punches and hedging bets (non-real problems, watered-down solutions, should this become a startup instead of a paper, …)
  - Ignoring reality: what is already solved in industry, or only solvable in industry
- **Clarity of purpose**
  - Strategically differentiating vs. Pre-competitive vs. Post-competitive
  - This is an industry-wide problem with defining the research agenda
- **Education**
  - Do students graduate with the ability to comprehend real product challenges and write high-quality software?
- **Software**
  - Incompatible, stand-alone optimizations

ABK Life Rule #34: You get what you incent

Where will they be attacked with the most success?

- **People Culture Clarity Education Software**
- **Open source, commodity components ideal of snap-on tools**
  - OpenAccess was an excellent ice-breaker
  - Need really free licensing models
  - Need correct valuation by universities, 3rd-best EDA companies
- **Research infrastructure**
  - Cell libraries (all views), DRMs, PDKs
  - Open-source HW (opencores.org, SPARC, etc.)
  - Up-to-date, pluggable implementation flows and methodologies
  - Problem definitions that come with data and solution evaluators
- **Education**
  - Develop people who are optimized for 21st-century EDA R&D

CAD Research, Pay Now or Pay Later...

ICCAD-2006 Monday Evening Panel

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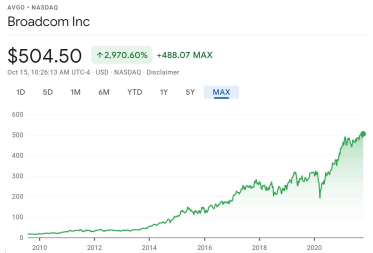
Those slides were from 15 years ago …

Two More Life Rules …

Learn from history (or be doomed to …)

- **What works**
  - **Being the beacon of opportunity for talent and innovation !!!**
  - Knowing it's a **marathon**, not a sprint: "long game"
- **What doesn't work**
  - Pushing on ropes, short attention spans, throwing $$$ without fixing root causes



Remember the Serenity Prayer

- **Accept what we cannot change**
  - Companies, students, faculty **all behave rationally in their reward systems**
    - **Semi:** consolidate, outsource, offshore, spin off, drop off leading edge, …
    - **EDA:** EULA terms, IP assertion, price/limits of University Program, #SolvNet logins for Michael, …
- **Change what we can**
  - Hierarchy of importance — **don't boil the ocean**; have lifeboat tests
  - Work backward from the end — always be on a **feasible** path
  - Culture change is powerful — academic credit/value assignment; tech/org health
  - Accountability and metrics — measure to improve; fool me twice, shame on me

Q: Do Goals Need Clarification?

Statement of Need:

Chip design at US universities blossomed on account of the Mead and Conway Revolution (Conway). In 1978-79, Carver Mead and Lynn Conway wrote the seminal textbook *Introduction to VLSI Systems* (Mead). This book offered abstractions that transformed digital chip design from a complex physics problem into a much easier computer science problem and popularized chip design in academia. Conway also taught a VLSI course at MIT in 1978 leading to the Multi-Project Chip concept, and Danny Cohen established the Metal Oxide Semiconductor Implementation Service (MOSIS) at USC for VLSI prototyping. MOSIS fabricated free chips for university VLSI classes, initially with NSF support and later with profits from their commercial operations, but ceased offering this service in 2020. DARPA also kicked off a VLSI research project in 1980, popularizing Mead & Conway's work and encouraging the development of chips and electronic design automation (EDA) tools.

Chip design was further fueled by a collaboration of universities and industry. Much early design was done with the MOSIS layout tool, but more advanced design requires synthesis and placement & routing tools. EDA vendors, including Cadence, Synopsys, and Mentor Graphics, established university programs with discounted tools. North Carolina State University developed the NCSU Process Design Kit (PDK) with modern predictive (i.e., non-fabricable) technology files ("FreePDK"). Through the 1990s, universities taught large VLSI classes at the graduate or advanced undergraduate level using a vibrant set of textbooks. Fabricating a chip through MOSIS and testing it became a rite of passage for thousands of engineering majors. Brunvand provided a cookbook to install and configure CAD tools and models for chip design with industry-standard tools on readily available processes (Brunvand). Flows became mature enough to be accessible to all university students.

In recent years, VLSI education has faced a decline leading to VLSI classes now offered only as a niche topic. According to faculty on a recent NSF-organized panel discussion, enrollments have dropped at most universities and the fraction of underrepresented students in these courses is close to zero at some schools. Textbook sales have sharply declined and predominantly moved to India and China. MOSIS has dropped support for the old 0.6-micron process long-used for class projects and dropped class funding entirely. The cost of discounted VLSI CAD tools is significantly higher than other university software and the cost per student increases when enrollments decline. The cost of maintaining these tools and their computing infrastructure also requires IT staffing and expertise as well as dedicated computer systems for licensing and installation.

VLSI research in academia has become very difficult because results using antiquated processes are generally not publishable and the design files (device models, design rules, and libraries) for advanced processes are proprietary and available only to faculty with special industry connections. Often universities are unwilling to sign the Non-Disclosure Agreements (NDAs) that some industrial partners require due to numerous restrictions on IP ownership, export control, liability, and other challenges. The cost of fabrication in advanced processes is also so high that it often requires piggybacking on an existing shuttle run from a corporate sponsor, again only available to faculty with special connections. Altogether, far fewer students are graduating from US universities who are prepared for careers in chip design.

The US is now facing both an economic and national security threat in the semiconductor industry. There is presently a worldwide semiconductor shortage that forced Apple to delay the iPhone 12 by two months ("Apple unveils new 5G iPhone 12 line in multiple sizes") and cost the automotive industry a forecasted $60B in revenue ("How Covid led to a $60 billion global chip shortage for the auto industry"). In 2014, Broadcom found itself unable to compete in the cell phone application processor market against foreign competition from Samsung and MediaTek, closed the entire division, and was weakened to the point that it was acquired by a Singapore company, Avago ("Avago Technologies to Acquire Broadcom for $37 Billion"). There is a multibillion-dollar black market in counterfeit electronics and an estimated 15% of spare electronic parts purchased by the US Defense Department are counterfeit, threatening both reliability and security ("Senate Hearing 112-340"). In 2020, the Federal Communications Commission designated Chinese telecommunication firms Huawei and ZTE as national security threats because of the risk of espionage through their 5G networking equipment ("F.C.C. Designates Huawei and ZTE as National Security Threats"). The Chinese National Integrated Circuit Plan seeks to develop leading-edge domestic integrated circuit manufacturing capability by 2030, and the country invested $150B in its industry between 2014 and 2020 ("Can China Become the World Leader in Semiconductors?"). In 2014, IBM sold their chip business to Global Foundries, ending a source of domestic chip manufacturing.

Several forces are coming together with prospects to revitalize the US semiconductor industry. In March 2021, Intel CEO Pat Gelsinger announced a $20B investment to build two new IC fabrication plants in Arizona for 7 nm manufacturing and to sell foundry services to outside customers ("IDM 2.0 is the Powerful Combination of Intel's Internal Factory Network, Third-party Capacity and New Intel Foundry Services"). This will significantly expand US manufacturing capacity. President Biden's "American Jobs Plan" of March 2020 calls for over $50B investment in domestic chip manufacturing ("Biden plans to connect every American to broadband in new infrastructure package"). The elephant in the room, however, how we will educate and establish a workforce to create designs for manufacturing in these fabs.

There has been a significant interest in how open-source hardware designs and EDA tools can impact IC design, which has been notoriously closed-source. DARPA has funded broadly the development of an entirely open-source toolchain ("UC San Diego Selected to Lead Development of Open-Source Tools for Hardware Design Automation"), and open-source FPGA tool flows have also seen very mature toolchains for multiple FPGA architectures ("SymbiFlow"). DARPA has also funded the Electronic Resurgence Initiative to secure the supply chain and promote integrated circuit research and development ("DARPA Chip Effort Pivots to Securing US Supply Chain"). The Free and Open Source Silicon Foundation (FOSSi) is promoting open-source EDA tools and libraries ("FOSSi"). Industry consortiums such as CHIPS Alliance have coalesced around such open-source opportunities ("CHIPS Alliance"). Google has recently begun sponsoring Skywater Multi-Project Wafer shuttles for any open-source project in older 180nm technologies and may expand to more recent, but still older, technologies ("Google Partners with SkyWater and Efabless to Enable Open Source Manufacturing of Custom ASICs"). One monumental success in the open-source area has been the adoption of RISC-V by numerous companies and academic institutions ("RISC-V grows globally as an alternative to Arm and its license fees"). Entire microprocessor ecosystems, which were once filled with proprietary ISAs, firmware, and compilers, are now freely available and competitive in performance.

While the Mead-Conway revolution began by moving IC design from analog designers to digital designers, the open-source movement may enable a shift from digital designers to software engineers for the next generation of "IC designers". Hardware design has benefitted from many software design efficiency and productivity paradigms such as high-level synthesis, intermediate representations, programming languages, formal verification, etc. Recently, for example, new high-level design languages such as Chisel have started to change how we abstract hardware design and offer new opportunities for optimization and integration ("Chisel/FIRRTL Hardware Compiler Framework"). Improved accessibility of open-source IC design ecosystems opens the opportunity for innovation as well as a chance to increase diversity by stretching the concept of who can be an IC designer.

As Moore's law diminishes, it is even more critical that universities reconsider their approach to IC education and research. Improvements in IC designs will need to come from new devices with disparate technologies, improvements in EDA toolchains and methodologies, and integration of heterogeneous systems. All of these will require rethinking both how we design to address the complexity and how we revitalize student interest in hardware systems. Academics and industry must address this change now when training our future workforce.

- Example: *In which organizations do we need to build the "workforce to create designs for manufacturing in these fabs"*?
- Should we clarify needs first, then goals?

Q: Can We Separate Concerns, Foci?

NSF Workshop Position Statements

Each position statement has 20 minutes total (strictly enforced for the equity of presenters. In your position statement, you should spend the first 5-10 minutes (no questions allowed) discussing your primary concerns and potential solutions. We will then follow up with 5-10 minutes of Q&A for discussion. For example, if you speak for 10 minutes there will be a limit of 5 minutes of Q&A. If additional time is needed, we will mark it as an item for discussion in the Q&A after the group of speakers.

To guide the discussion, we have some potential issues/questions. **Please consider the most important ones to you (you do not need to answer them all!). Please consider diversity and inclusion, existing resources, and areas of flexibility at the end as well.**

F…try/Government:

- …VLSI jobs within/outside the US, and what trends do we see at tho…
- …bring more of these jobs to the US?
- Wh… recruit and why?
- How do y… academic research funding, and…
- How important … ave specific components of
  - Intro and adva…
  - Device manufacturi…
  - Experience with contempo… rocesses
  - Commercial CAD tool experience
  - Team projects/large scale projects
  - Fabrication and/or testing experience
  - Scripting/Unix/Linux/System Administration
- What is missing from VLSI education?
- How can open-source hardware and EDA tools help?
- What are the problems with open-source hardware and EDA?
- How important is academic research to you?
- How can we provide support for start-ups? What incubators are available?

For Academia:

- How can EDA infrastructure be low cost and low maintenance?
  - Can you use Virtual Machine or Docker images?
  - Is licensing a problem? Floating licenses vs. fixed-node vs. unrestricted?
  - How can you manage confidential material in a safe way?
- What are server hardware and setup needs?
  - How to utilize student laptops vs. workstations vs. large servers vs cloud?
  - Is cloud computing feasible?
  - Are there needs for special hardware (GPUs, many-core, large…
- Education
  - What tools and features are missing?
  - What design models, PDKs, IP are needed…
  - What process nodes are adequate?
  - Are there different needs for…
  - What are the deficiencies … and EDA tools?
- Research
  - What advanced process nodes are needed?
  - What level of technology details is adequate?
  - What manufacturing information is needed?
  - Do you need partially processed CMOS wafers for further in-house processing?
  - Do you need wafer information for yield/analysis?
  - How to collaborate and fund fabrication?
  - What is needed for post-Moore technologies?

For all:

Diversity and Inclusion:

- How can we increase hiring pools?
- How can we build a community college pipeline?
- How can … rease undergraduate enrollments?
- How can … raduate enrollments?
- How ca… tment to improve diversity?
- How ca… more inclusive?

For all:

Existing resources: How are the re… equate? What must be changed to make them adequate?

- MPW shuttles
- Cost of fabrication
- Predictive technologies and PDKs: (e.g. FreePDK, …AP, PTM)
- Open-source, manufacturable P…Ks (e.g. Skywater130)
- Availability of design co… research and fabrication
- Open-source desig… ols
  - ISA…
  - …
  - …ws (OpenRoad, OpenLane, gEDA, etc.)
- Other…

For all:

Areas of flexibility: What areas can we make compromises?

- Can fabrication companies make models and PDKs available to a broad set of universities under NDA?
- Can EDA … gine a way to have their tools on a centralized server, reduce needs for NDAs, … cost of ownership?
- Can open-s… st and difficulty of maintenance of commercial tools while providing the sam… benefits?
- What design collateral … ilable to participating universities?
  - Cell libraries, memory … ors, peripherals?
  - Chiplets ("fill in the blank" …
- Can open-source IP be used instead of com…
- Access to fabrication for universities:
  - What technologies are sufficient?
  - How should the available technologies be updated ov… me?
  - How should it be funded and managed?
- How can recruiting pathways from universities to companies and startups be facilitated?
- Can the research and education infrastructure be extended to help startups?

Yes to cloud, containers!

How will progress be measured? (KPIs)

How can we replicate and scale known successes?

Solution exists: just add $$

"Not a hill to die on"

Flexibility of skills, learning how to learn, curiosity for a lifetime …?

"your primary concerns and potential solutions" □ maybe collect offline?

Would Like To See

- **1. Don't lose "north star" = what led to U.S. success**
  - **Attract the best talent, provide the best opportunities for innovators**
  - **(learn from leading programs, exemplars)**
- **2. Do better**
  - **Faculty**
    - **Share** solutions, precedents and existence proofs (NDA/LUL terms, course infrastructure, COVID-19, …) Slack ☺
    - **Share** education technology (MSE 2.0)
    - **Share best practices for sharing** ☺
    - Rise above that (#*&!(*!) bean-counting do the right thing (open-source, share, …)
    - BTW: EDA companies are great here: training courses, RAKs, web portals, cloud offerings, …

Shout-Out + Thanks to EDA Vendors …

- **How CAD research with vendor tools became reproducible after all …**
  - *Hi, Andrew – my students want to replicate your studies in paper XXX. We have the ASAP7 but how exactly did you run the YYY tools? Thanks, Bora.*
  - *Hi, Bora – No problem. But please send me a note confirming that you and your students are currently licensed users of the YYY tools (e.g., under relevant paid-up subscriptions to vendor University Programs).*
  - *Hi, Andrew – Sure thing – here you go: I confirm that I and my group members are all currently-licensed users of the YYY tools via a current subscription to the YYY University Program.*
  - *Hi, Bora – Thanks … can you also send me GitHub handles? We'll give access to a private repo with the relevant runscripts + public testcases. Note from the paper that we used vZZZZ.Z !*
    - *// Alternative: explicit sharing of Drive account*
    - *// Alternative: .htdocs/.htpasswd at a (transient, dark) URL*
  - *Hi, Andrew – got it, we're good to go.*

  - Comment 1: From O(N) to O(1) sharing effort: EDA vendors can also put your scripts behind their access-controlled portals (pipecleaners in 2018)
  - Comment 2: Hammer, CADRE, mFlowgen, … (Tcl bytecode?) are bases of other mechanisms
  - Comment 3: This **could** be less cumbersome but **IMO it's a solved problem much happier now**

- **Support of student learning and research**
  - **University Programs**
  - **Generic PDKs**
  - **Real training classes, RAKs, recent tool versions, …**
  - **Pandemic** "Recognizing that the extraordinary travel and congregation restrictions imposed as a result of the novel coronavirus (COVID-19) calls for extraordinary measures, notwithstanding the terms and conditions of the applicable license agreement, YYY agrees that for 90 days, …"

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    - **Share** education technology (MSE 2.0)
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    - Rise above those #*&!(*! bean-counters do the right thing (open-source, share, …)
    - BTW: EDA companies are great here: training courses, RAKs, web portals, cloud offerings, …
  - **Government**
    - Fund long-term, stable **infrastructures** including supply chain + professional staff
      - VLSI design (tooling, expertise) + fabrication + packaging, test (multiple regions do this)
      - **Advanced devices and structures/fabrics, not just mainstream**
    - **Define** the democratization goal (e.g., open and equal access?)
    - **Fund more "engineering"** to build systems, along with translational, innovation efforts ("TIP"?)
    - Broadly incentivize ($$$) creation and support of high-quality shared **infrastructure** (IP, labs, …)
- **3. Accountability**

Messages

- **This is a great workshop – thanks to the organizers**
  - The talks and discussion have been wonderful
  - Harness energy, good will, sense of collective mission
  - Clarify needs, purpose, goals, boundary conditions, …
- **Don't lose sight of how VLSI Design in the U.S. had such incredible success**
  - Share successes, lift all boats (vs. "common denominators")
  - Flexible skills, fundamental knowledge, …
  - Beacon to talent worldwide, best environment for innovation
- **What is different this time around?**
- **If it's meaningful, it will be a marathon**
- **"How can I help?"**

THANK YOU !

(Q&A)

Backup: Misc + Perspective

- *Company* **funding tapeout classes at Stanford, Berkeley, CMU is great**
  - Multiple *companies* are joining this trend !

- **Gradients are really tough**
  - Best talents (foreign and domestic) want to do other things than hardware
  - Brain Drain: "biggest threat to EDA is Google" - Igor Markov, 15 years ago (see #5)

- ***Perspectives / Retrospectives***

1. "CAD Research: Pay Me Now or Pay Me Later", ICCAD 2006 (slides)
2. "Toward New Synergies Between Academic Research and Commercial EDA", CDNLive 2016 (slides)
3. "A 'Life Cycle' of Teaching and Research on EDA and IC Implementation Methodology", CadenceLIVE! 2020 (slides, mp4)
4. "Open-Source EDA: If We Build It, Who Will Come?", VLSI-SoC 2020 (slides, mp4)
5. About brain drains: 2004 EDA Confidential interview

Misc: Flows (CadenceLIVE, August 2020)