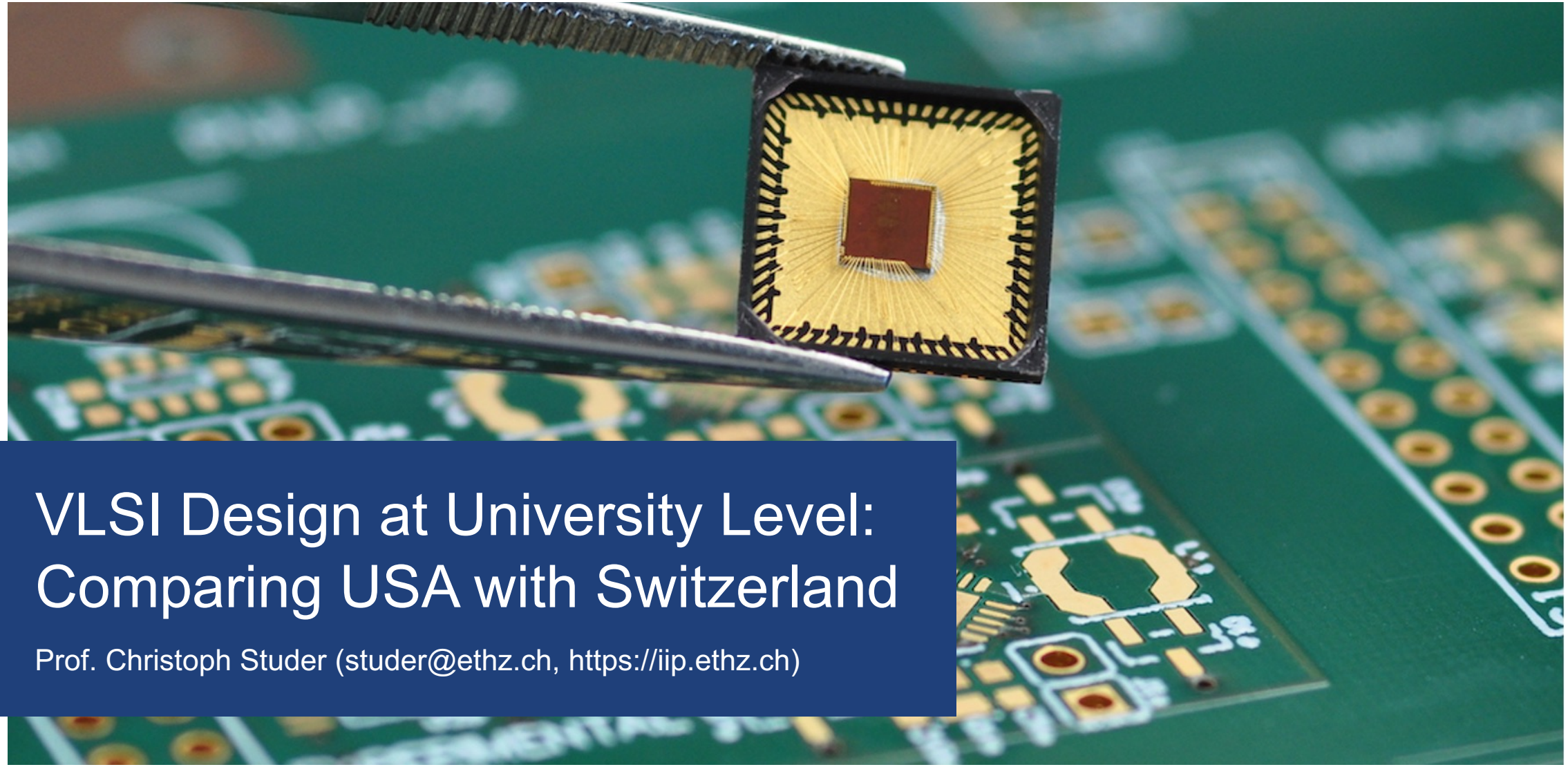
Integrated Information Processing (IIP) Group
Integrated Systems Laboratory

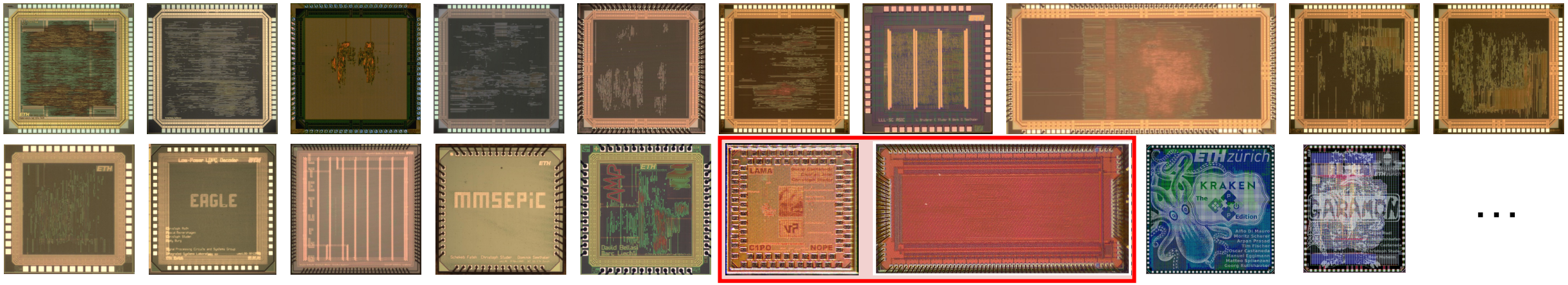


VLSI Design at University Level: Comparing USA with Switzerland

Prof. Christoph Studer (studer@ethz.ch, https://iip.ethz.ch)

About me – Prof. Christoph Studer

- 2000-2009: Undergraduate studies, MS, and PhD at ETH Zurich
- 2009-2013: Postdocs at ETH Zurich and Rice University
- 2014-2019: Assistant Professor at Cornell University
- 2019-2020: Associate Professor at Cornell University and Cornell Tech
- Since June 2020: Associate Professor at ETH Zurich



Disclaimer

- This is more of a comparison between Cornell University and ETH Zurich
- This comparison is based on my own experience
- This comparison is **not** complete

University funding

Cornell University

- School of Electrical and Computer Engineering (part of the College of Engineering) is private

ETH Zurich

- Federally funded

Teaching

Cornell University

- Introduction to Digital (VLSI) Design (ugrad.)
  - Full-custom digital circuit design
- Complex Digital ASIC Design (graduate level)
  - Tool-based ASIC design with PyMTL

ETH Zurich

- VLSI 1 (undergraduate level)
  - HDL-based design for FPGAs
- VLSI 2 (graduate level)
  - Tool-based SoC/ASIC design (+ tapeout)
- VLSI 3 (graduate level)
  - Full-custom digital circuit design
- VLSI 4 (graduate level)
  - Measurement and testing

- Applied Circuit and PCB Design (ugrad. level)

VLSI design

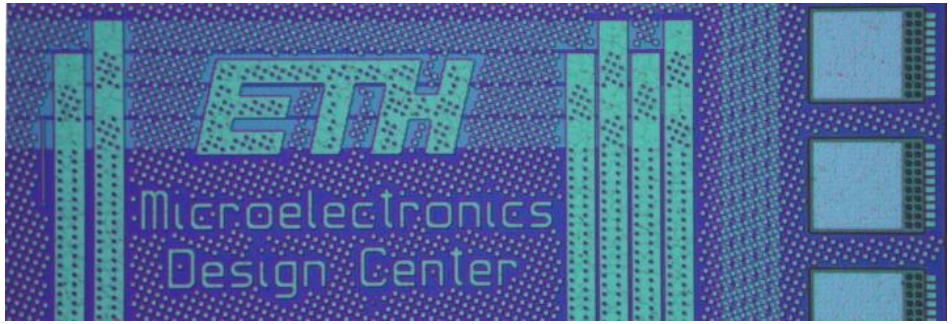
Cornell University

- CAD tools, licenses, and PDKs installed and maintained by professors and Ph.D. students
- NDA and PDK access handled by professors
- Compute and CAD servers owned by individual professors (some shared in CSL)
- Tapeout via, e.g., Muse Semiconductor
- PCB design and assembly by Ph.D. students
- Testing equipment set up with, e.g., pattern generator and logic analyzer
- Funding from grants or gifts

Computer Systems Laboratory (CSL)

VLSI design

https://dz.ee.ethz.ch



DZ Team Summer 2021



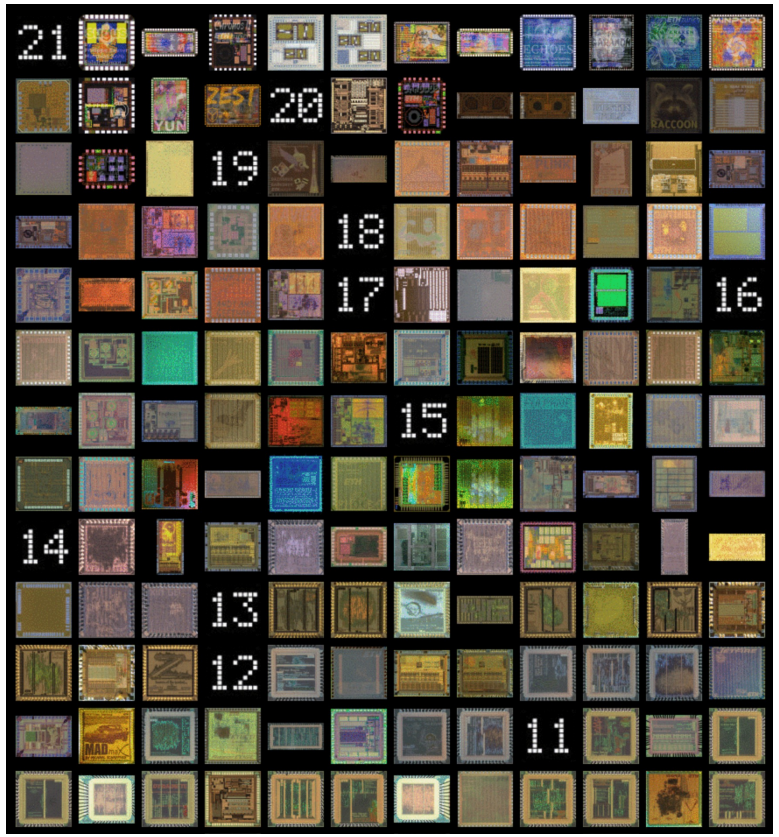

ETH Zurich

- Microelectronic Design Center (DZ)

  “To provide design tools, know-how and licenses for ASIC, FPGA, Embedded Systems, and PCB design for research and teaching”

  - 4 full-time employees (non-research)
  - Maintain CAD tools, licenses, PDKs
  - Deal with NDA and export-control aspects
  - Support submission procedures
  - Design PCBs, including assembly
  - Support teaching for VLSI 1-4 lecture series

VLSI design (cont'd)



http://asic.ethz.ch

ETH Zurich

- Microelectronic Design Center (DZ)
  - Over 500 ASIC tapeouts since 1986
  - About 5-15 chips per year
  - Many well-supported technologies with recent tapeouts (GF22FGX, GF45SOI, TSMC40LP, TSMC65, UMC65, etc.)
  - Some technologies available for design, but not fabrication (TSMC7, ALP180, etc.)
  - Testboards for many different packages (QFN40/56/64/88, BGA169, PGA120, etc.)


ETH zürich
KRAKEN
The
P
Edition
Alfio Di Mauro
Moritz Scherer
Arpan Prasad
Tim Fischer
Oscar Castaneda
Manuel Eggimann
Matteo Spllanzani
Georg Rutishauser


ETH zürich
KRAKEN
The
P
Edition

VLSI design (cont'd)

Advantest SoC V93000

ETH Zurich

- ASIC Tester: Advantest SoC V93000
  - 256 digital channels up to 1.6Gb/s
  - 64 channels up to 9Gb/s
  - Analog and RF options
  - Used to test student designs in VLSI 4
- Servers provided by professors and maintained by Integrated Systems Laboratory
- Tapeout funding provided by ETH Zurich (up to $100k per year per professor)
- Separate funding by D-ITET/DZ for student tapeouts as part of the VLSI 2 lecture

Challenges

Cornell University

- Dealing with NDA and export control issues
- PDK and tool maintenance overhead
- Continuity if PhD students leave → one needs to maintain a relatively large group
- Difficult to get funding for (student) tapeouts

ETH Zurich

- Student diversity
  - Only very few female students (<15%)
  - Large portion of students taking VLSI 1-4 are MS students from Asia (who leave)
- Excluded from US/EU funding opportunities

- Access to cutting-edge packaging options

Questions?