Standing Up an Academic MPW to Enable IC Design Education

LaMar Hill

President's Office

NY CREATES

Supporting NY, US & Global Semiconductor Ecosystem

Douglas Grose Ph.D.
Chairman

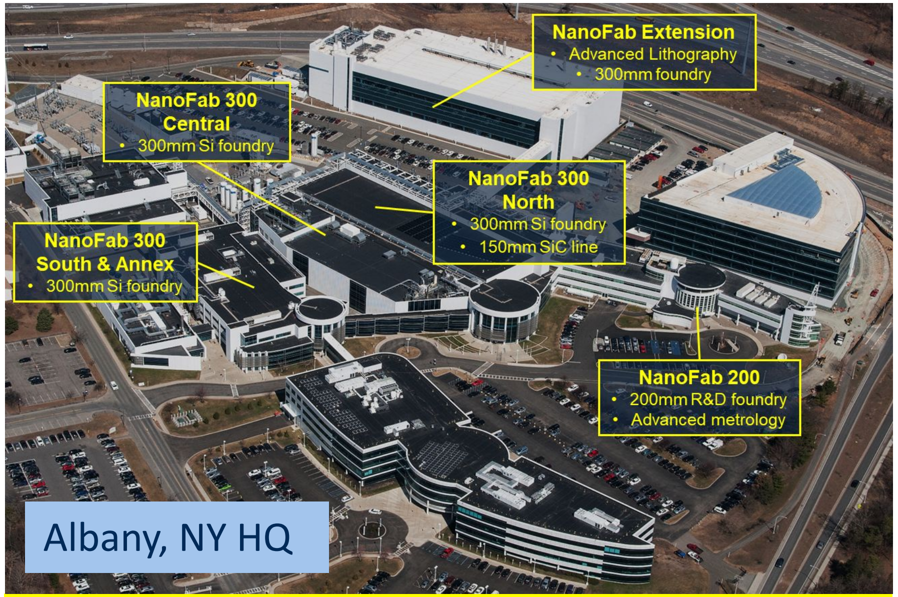
Primary Stakeholders

- New York State
- US Government
- Industry
- SUNY RF

ONGOING PROGRAMS

- NY CREATES-CSR 300mm R&D FOUNDRY
- APPLIED MATERIALS META CENTER
- TEL TECHNOLOGY CENTER AMERICA
- NY PEMC[1] (CREE, DANFOSS)
- IBM AI HARDWARE CENTER
- ROCHESTER TAP[2] FACILITY
- AIM PHOTONICS

[1] New York Power Electronics Manufacturing Consortium
[2] Rochester Test, Assembly, & Packaging



- Greater than $15B Investment
- 2,700 Staff, Scientists & Engineers
- 164k ft^2 Clean Room Space
- More than 200 Industry Partners
- $350M/year Operating Budget
- $150M/year Cap-Ex Equipment Budget

LaMar Hill President's Office
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Primary Services

- Technology R&D
- Economic Development & Commercialization
- Workforce Development

ONGOING R&D

- AI/NEUROMORPHIC COMPUTING
- INTEGRATED PHOTONICS
- QUANTUM TECHNOLOGIES
- EMERGING MEMORY PLATFORMS
- POWER ELECTRONICS
- NANOBIO DEVICES
- HETEROGENEOUS INTEGRATION

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https://ny-creates.org

Major Initiatives Timeline

08/98
SIA Semiconductor Industry Association

07/02
SEMATECH
International SEMATECH North ($320M/5 years)

04/04
College of Nanoscale Science & Engineering, University at Albany, State University of New York
College of Nanoscale Science & Engineering Formed

01/05
IBM

IBM-Albany CSR ($450M)

06/06
AMD, GlobalFoundries
GF – Luther Forest Plant ($12B)

07/08 ★
IBM
$1.5B Packaging R&D & MFG

02/10
G450C Manufacturing Initiative ($4.4B/5 years)

11/18
Applied Materials make possible
META Center $850M/7 years

9/19
CREE Wolfspeed
PEMC & Marcy Nanocenter $1.7B

04/01

Nanoelectronics Center of Excellence ($150M)
IBM

11/02
Tokyo Electron Ltd. (TEL) Technology Center America
TEL

01/05
ASML R&D Center ($400M/5 years)
ASML

07/05
INVENT ($600M/7 years)
Micron

05/07
International Sematech / NYS Agreement ($300M/5 years)
SEMATECH

07/15
American Institute for Manufacturing Integrated Photonics ($600M/5 years)
AIM photonics

01/19
IBM Research AI Hardware Center ($3.2B/5 years)
IBM

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The Grand Workforce/Talent Challenges

- Severe lack of Qualified Construction Workers
- Semi Industry’s “Career Path Appeal” for Chemists, Chemical Eng, EHS Eng, Mech Eng., Electrical Eng., etc.
- Disconnect between Industry & Educational Systems
- Academic Silo-ing
- Diverse Regional Workforce Dev. Systems
- **Greatest Challenge Filling the Seats**

Academic EE & IC Design Education & Research Efforts in NY & US

New York University Partners

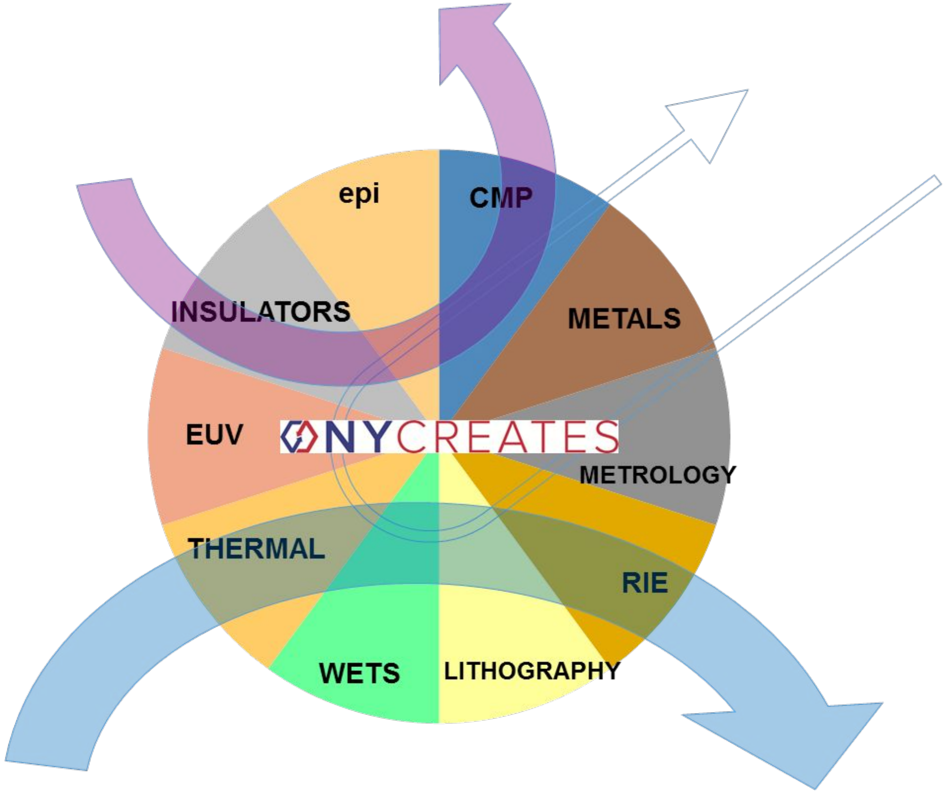
- **Cornell University**
- **Columbia University**
- RIT
- URochester
- RPI
    - CCNI
- NYU
- Clarkson University
- Westpoint-The Military Academy
- Syracuse University
- SUNY
    - Poly/CNSE, U Buffalo, Stony Brook, Binghamton
- **NY Output of EE with Design Focus 800/year**

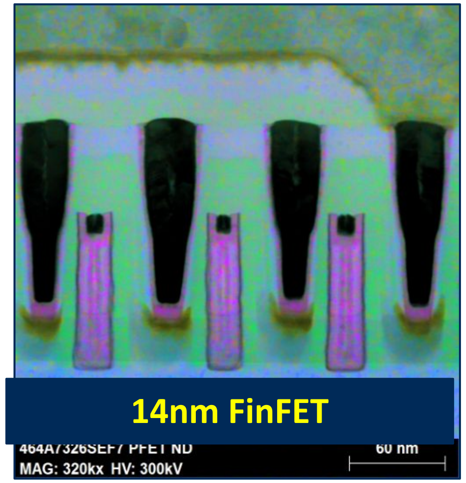
Traditional US University Relationships

- MIT
- UCSB
- U Arizona
- Purdue
- UT Knoxville
- U Maryland

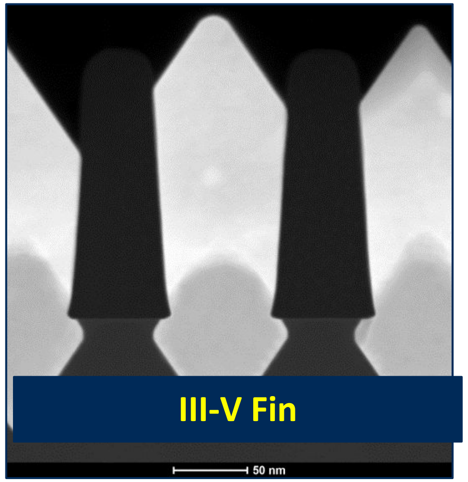
300mm R&D Fab

- Industry technology, equipment and supply chain leaders leverage the state-of-art fab
  - 65 nm Base Full Flow, Advance nodes available downstream, R&D on 7nm to 2nmga
- NY CREATES team provides:
  - Process development across all sectors
  - Integration and data analysis
  - Includes Test Assembly & Packing along with Heterogeneous Integration
  - MPW Management
  - Operational execution
  - Flexible work scope

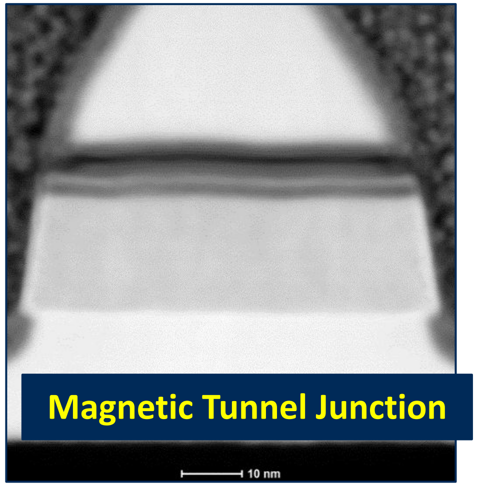




14nm FinFET



III-V Fin



Magnetic Tunnel Junction

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Organizational Experience with MPW Runs

- There has been a Photonic IC MPW in place for 5 years using base 65nm IBM initiated process with CMOS PDK.
- A PIC PDK was developed and for first 2-years Aggregation and admin was done by MOSIS.
- Last 3-years entire effort done by in-house engineering staff
- Typically 3-4 MPW runs are completed each year.

Standing Up a NY CREATES Academic MPW

- Vision
  - Start with 65nm full Flow with open PDK
  - Up to 20 Universities get a tile allowing multiple designs for each reticle-mask set
  - NY CREATES to complete aggregation/tape out with maximum learning for all.
  - Expect multi-semester program with Fab effort, evaluation, test in last semester of program
  - Initial program would be Front end Si Run
  - Advanced Packaging and Test added on.
  - Fund Raising and Program development with Founding Universities Jan-Sept. 2022

New Thrusts in IC Design

- Academic MPW Summit spring 2022
- Partnership with Synopsys, Siemens-Mentor Graphics, Cadence, ARM
  - Access to IP Library
- Joint University Delivered IC Design Curriculum
  - Certificate Programs
- Design Center Of Excellence for RF, DoD, Bio Chips, Autonomous Ops and Energy Chips at Primary Research Universities
- Partner with Industry through SRC & SEMI
- Internships & Engineering Co-ops a MUST

Get Involved!

- Your Input is much needed! We are open to ideas!
- Let’s re-invigorate the ubiquitous IC Design Cycle

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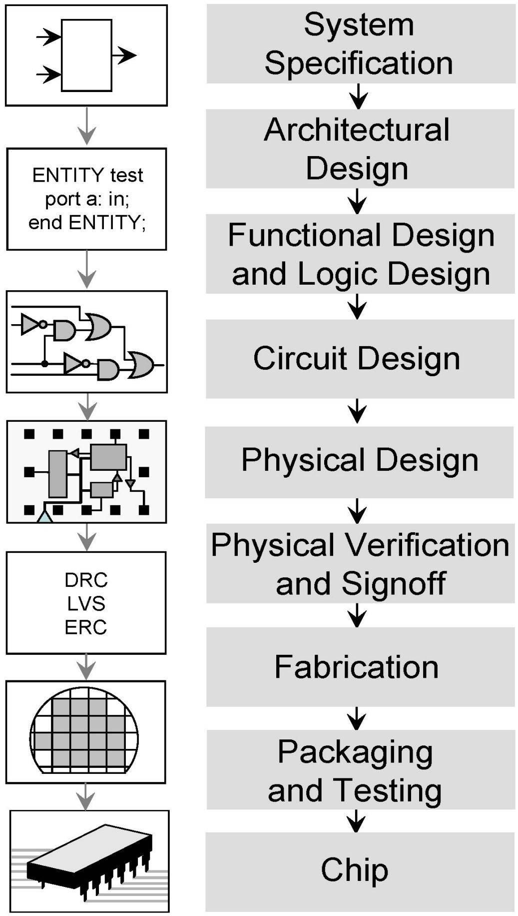

System Specification

Architectural Design

Functional Design and Logic Design

Circuit Design

Physical Design

Physical Verification and Signoff

Fabrication

Packaging and Testing

Chip