Michael Taylor, University of Washington

I love building new kinds of chips that break world records, and open sourcing the entire system from RTL to Package to PCB and Firmware.

BaseJump: Building the DNA For Open Source ASIC Systems

Brought to you by Taylor's Bespoke Silicon Group.

Our vision is to create a path that allows researchers to prototype their ideas without worrying about all of the intricacies of I/O, packaging, PC board design and FPGA coding.

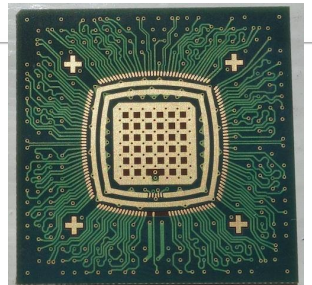
Our goal is to shave 10-15 people-years off of a typical ASIC prototype development process, and at the same time enable artifacts that are of superior performance to what most research groups would have the resources to do.

We have implemented a complete system that extends from the pad ring of the chip all the way out. You just need to design your verilog to connect to our simple interface, and then make use of the pre-built components that we have developed and tested. Push it through IC Compiler, PrimeTime and Calibre to a tapeout. The rest of the way has already been thought out.

Current Users:

University of Washington
University of Utah
University of Toronto
Princeton University
University of Illinois Urbana Champagne
Massachusetts Institute of Technology
University of California, San Diego
U of Cambridge
Cornell
U. Michigan

Prof. Michael Taylor
Bespoke Silicon Group
University of Washington CSE and EE



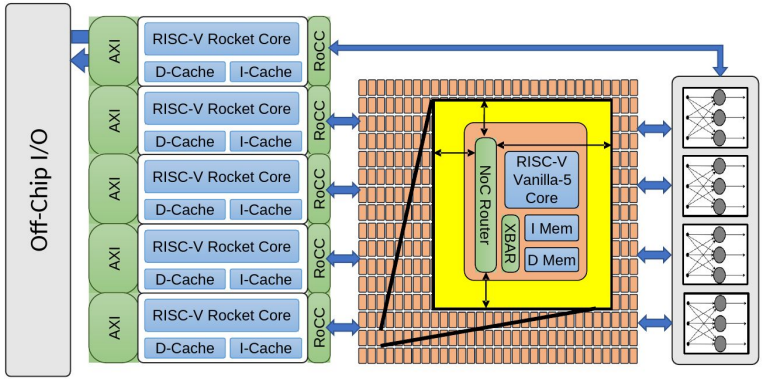
BaseJump Projects

BaseJump STL for SystemVerilog
BaseJump Manycore
BaseJump ASIC Sockets
BaseJump ASIC Motherboards
BaseJump FPGA Bridge
BaseJump RoCC Doc
RV-IOV: RISC-V IO Virtualization

All on github

BlackParrot

Open source Linux Capable
RISC-V Multicore



511-core 16nm RISC-V Celerity Chip
Broke world record for RISC-V performance
By 100X In 2017

It is little wonder that our VLSI pipeline in the US is atrophied

Every VLSI professor has to be a hero and make miracles happen

Negotiating export control and NDAs

Shaking trees to get funding for fab slots (NSF CCF (architecture) will not fund tapeouts)

Getting access to fabs (mostly about the prestige of your institution and the fame of professors)

Find a way to pay for commercial tools for student classes and bring up a flow for them

Getting access to packaging

Getting fab runs pulled

Large companies like Apple, and NVidia hire our students but provide no support for VLSI pipeline

Apple Market cap: $2.3T

Nvidia Market cap: $0.5T

Despite our efforts, Is the situation getting better or worse? (Frog in boiling water analogy?)

Maybe it is not an accident that we have the problems we do

Globalization & *comparative advantage* is working against us.
Other nation's educational pipelines (india, china) are feeding US industry via US Uni M.S. → H1B

While Smart US citizens focus on
more lucrative areas:
.. ML
Software for Ads
Medical Care

Does the US government and industry need to remove roadblocks if they want to avoid what happened to manufacturing happening to VLSI for supply chain / security reasons?

Maybe US $ that goes to the semi industry should require them to provide services for Universities to keep the educational pipeline in tact? (sort of like DoD SBIR's)

Baseline need for academic architecture/VLSI research

- **Stable access (5+ years per NDA signed) to FinFET PDK**
  - Getting NDAs signed by university takes literally hundreds of emails and many round trips
  - TSMC year-long lockouts on switching technologies..ugh; Export control limiting Chinese and Iranian students very problematic.
  - MOSIS routinely cancelled our TSMC access with literally 0 days of notice after spending months of my life on these contracts.
  - Chip design professors are at a fundamental disadvantage in academia because tenure committees do not allow you to put NDAs on your publication list =)
  - Need to be able to update student lists.

- **Stable 5-year promise of once a year tapeouts in the same technology**
  - Maybe alternating 3x3 mm and 6x6 mm
  - I have had 3 different foundries cancel promised tapeouts -- devastating impact on students & waste of time.

- **Similar stable access to modern DDR PHY and Controller for prototypes**
  - Digital chips are not realistic without some kind of memory system
  - I/O can be done at 1.1 Gbps/pin with standard LVCMOS I/Os with BaseJump so it's not usually a barrier

- **Commercial enablement for that PDK and FULL ACCESS TO documentation for IC design tools**
  - Synopsys had a rule that only two students at university can access Solvnet -- recent improvement: research groups can have a list of students w/access

- **About 6 students of funding per year**
  - Building chips has many steps (packaging, pcb design, CAD flow configuration, etc) and many expertises that one student can not be an expert in and complete a PhD
  - Need to distribute expertise and "create a pipeline" and sustain a 1-2 chip/year cadence to keep the knowledge in the group

I have weak approximations of these today; but only because DARPA MTO brokered the access as part of the SDH/POSH program (**thank you!**).
NSF provides none of these. Cloud does not actually solve any of these problems.

New things could help accelerate innovation

- **5 yr Access To Silicon Interposer and Microbump Assembly Technology**
  - Currently this is much harder to get access to than an MPW run
  - Because of this, it is not currently a democratizing technology, even though it sold that way
  - **If academics had widespread access to this, they could self organize and build a chiplet ecosystem and this would be extremely powerful and create huge innovation.**

- **5 yr access to package substrate fabrication technology**
  - Academics are locked out of a lot of innovation because they cannot play with substrates
  - E.g. design multi-chip modules, packages, etc; like AMD recent decomposition of X86 into multiple chips

- **5 yr access to on-package photonics**
  - Super hot area limited by access

- **Free sharing of PDK and CAD Flow scripts between academics who signed the NDAs, without yet another legal agreement that has to be signed.**

Open Source: categories & what can be sustained in academia

- **Software or IP that have concrete specs, does not need to evolve and can be finished and put on a shelf.**
  - I.E. burst of funding, students work on it, finish it, project is mothballed, student graduates
- **Software or IP that can be decomposed into half-person blocks (or smaller) that can be designed with concrete specs and little co-design required between blocks**
  - Larger than this, no new PhD student want to or be able to take it over when a student leaves
  - Still will need sustained academic funding to keep it alive
- **Things that need to evolve and cannot be decomposed will need sustained funding and professional teams in order to maintain**
  - E.g. RTL-to-GDS

Cloud -- only works if it is free and we have root

Configurations are way overpriced versus in-house machines.

Machine configurations are suboptimal.

Control over the machine is very important.

Our last tapeout would have been $450,000 of AWS credits,
more than the cost of our machines for only 3 months of use.

The overhead of maintaining the flow will not disappear with the cloud.

Lots of bugs need to be fixed in the PDKs over time; a static unsupported PDK will not work.

Installing tools is not the problem; this takes about 6 hrs per year for a busy grup using many tools.

Education / Open Source / Old Nodes

Open source PDKs seems very exciting to address export control, NDAs

The frustration of CAD tool usability impacts course reviews and student perceptions of VLSI

Open Source CAD tools currently require more support than closed source tools and would need more investment to achieve "frustration parity" with closed source tools.

Old nodes: to be exciting to students, they should be able to do something that a $250 Xilinx Ultra96 16nm FPGA board cannot do.

ETH Zurich has a robust educational pipeline with tapeouts funded by the dept on advanced nodes: 500 chips! Maybe a model to look at for the US.

ABET Stranglehold

On Early ECE Education

Hurts Digital VLSI

5 Math, 1 Chem, 2 Phys

Sample 4-year schedule for DTC Students Largely unneeded by digital VLSI

Freshman – Autumn Quarter		Freshman – Winter Quarter		Freshman – Spring Quarter		Yr tot	
Math 124 – Calculus I	5	Math 125 – Calculus II	5	Math 126 – Calculus III	5		
Chem 142 – Chem & Lab I	5	Phys 121 – Mechanics & Lab I	5	Phys 122 – Electro & Lab I	5		
E-FIG: Engr 101 & Gen St 199	2	VLPA/I&S	5	English Composition	5		
VLPA/I&S	5						
Quarter Total	17	Quarter Total	15	Quarter Total	15	47	
Sophomore – Autumn Quarter		**Sophomore – Winter Quarter**		**Sophomore – Spring Quarter**			
Math 207 – Diff. Equations	3	Math 208 – Matrix Algebra	3	CSE 143 – Comp Prog. II	4		
Additional Science or Math	4	CSE 142 – Comp Programming I	4	VLPA/I&S/DIV	5		
Additional Science or Math	5	Elective	5	Elective	5		
Elective	5	Elective	5				
Quarter Total	17	Quarter Total	17	Quarter Total	14	48	
Junior – Autumn Quarter		**Junior – Winter Quarter**		**Junior – Spring Quarter**			
EE 215 – Fundamentals of EE	4	EE 393 – Adv Tech Writing	4	EE 201 – Computer HW Skills	1		
EE 241 – Python & Skills	2	EE 242 – Signal Processing 1	5	EE 280 – Exploring Devices	4		
EE 271 – Digital Logic & Comp.	5	Advanced ECE Elective (Pro Iss)	1	Advanced ECE Elective	4		
Engr 231 – Intro Tech Writing	3	VLPA/I&S	5	Statistics	3		
Quarter Total	14	Quarter Total	15	Quarter Total	12	41	
Senior – Autumn Quarter		**Senior – Winter Quarter**		**Senior – Spring Quarter**			
Advanced ECE Elective	4	Advanced ECE Elective	4	Advanced ECE Elective	4		
Advanced ECE Elective	5	Advanced ECE Elective	5	Advanced ECE Elective	5		
Advanced ECE Elective	4	Elective	5	VLPA/I&S	4		
				Elective	4		
Quarter Total	13	Quarter Total	14	Quarter Total	17	44	180