

# Welcome

## IC Research, Education, and Workforce Development Workshop



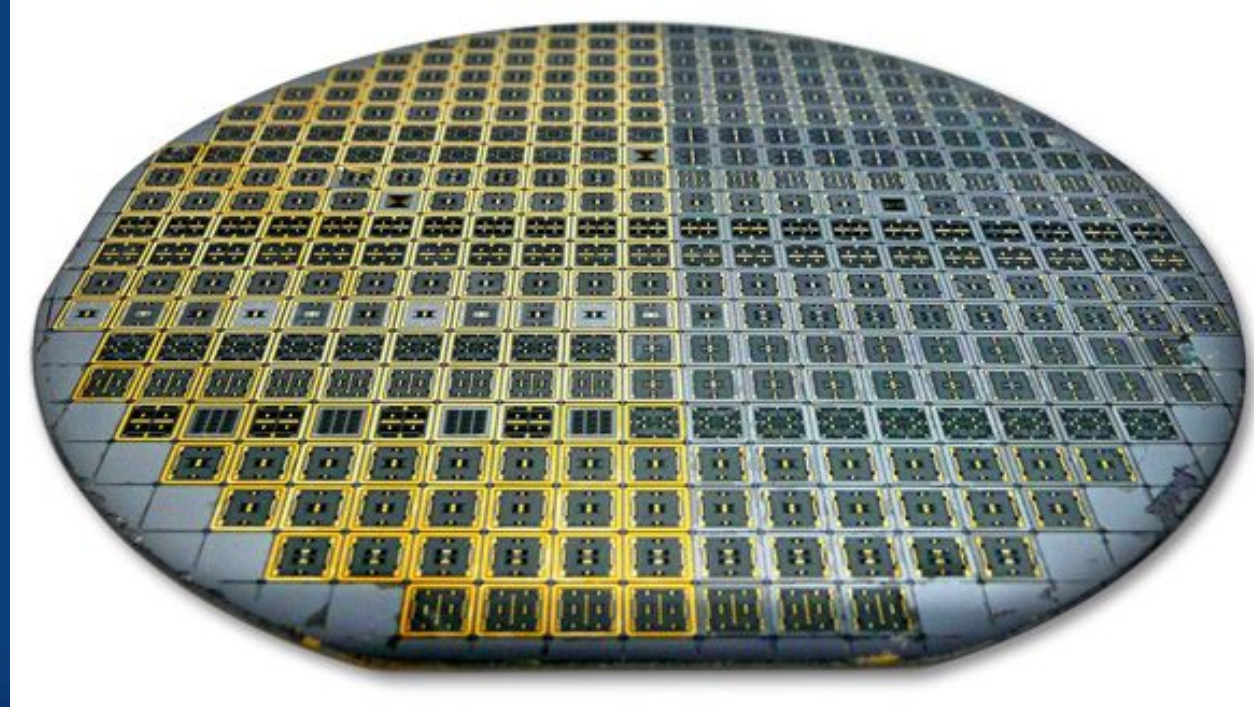
Erik Brunvand  
CISE/CNS  
October 2021





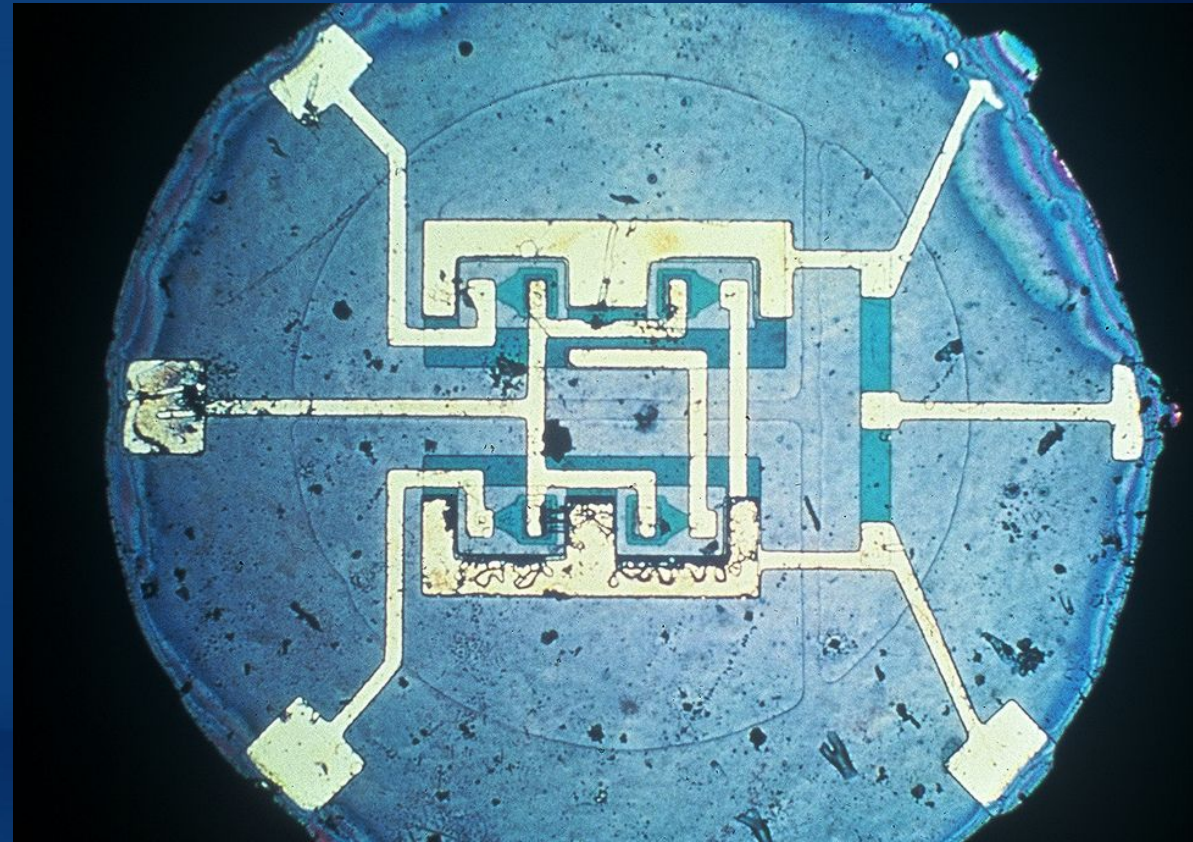
# Welcome from NSF

- The outcome of this workshop will hope to provide future guidance on the shortage of IC design engineers in the US and training a future workforce. In particular, the workshop will examine industry and academic needs to find the appropriate pathway for the revitalization of IC research and education in the US.



# NSF: Beyond the Current Roadmap...

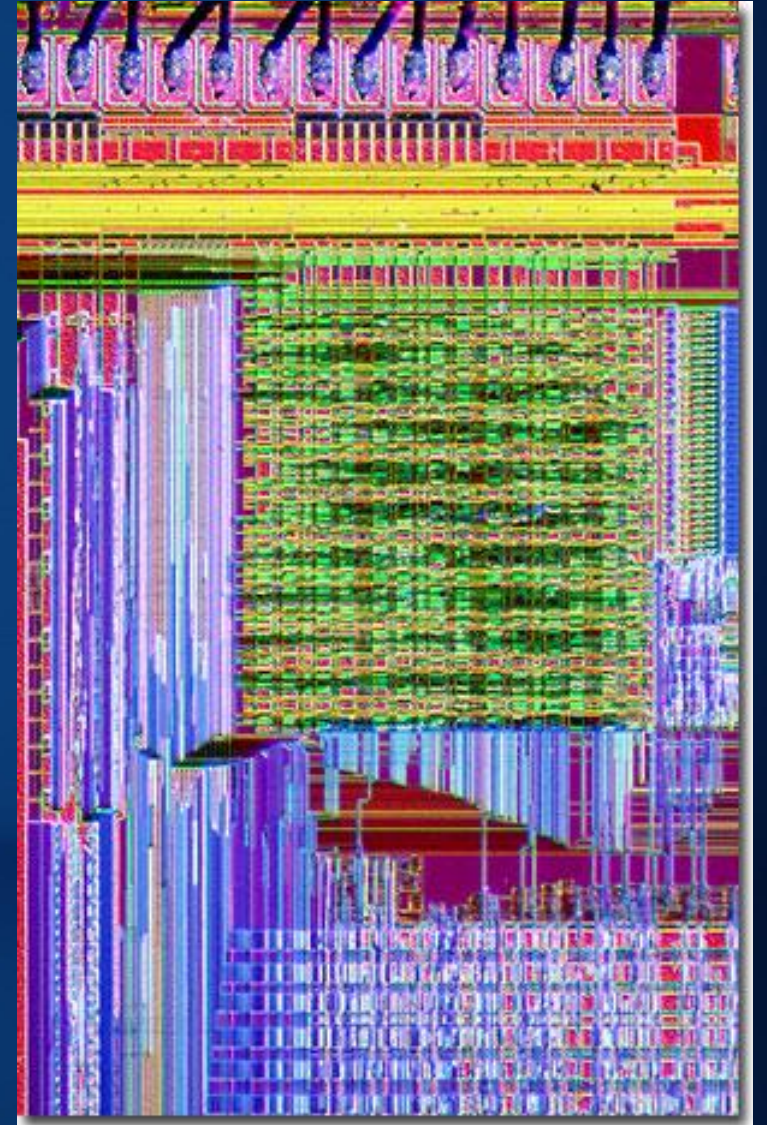
- Challenges in semiconductor and microelectronics due to the impending end of Moore's law create opportunities for the post-Moore's-Law semiconductor-based systems
- While many semiconductor-related challenges have loomed for some time, the topic is now in new prominence, and NSF has an opportunity to lead on important new research investments





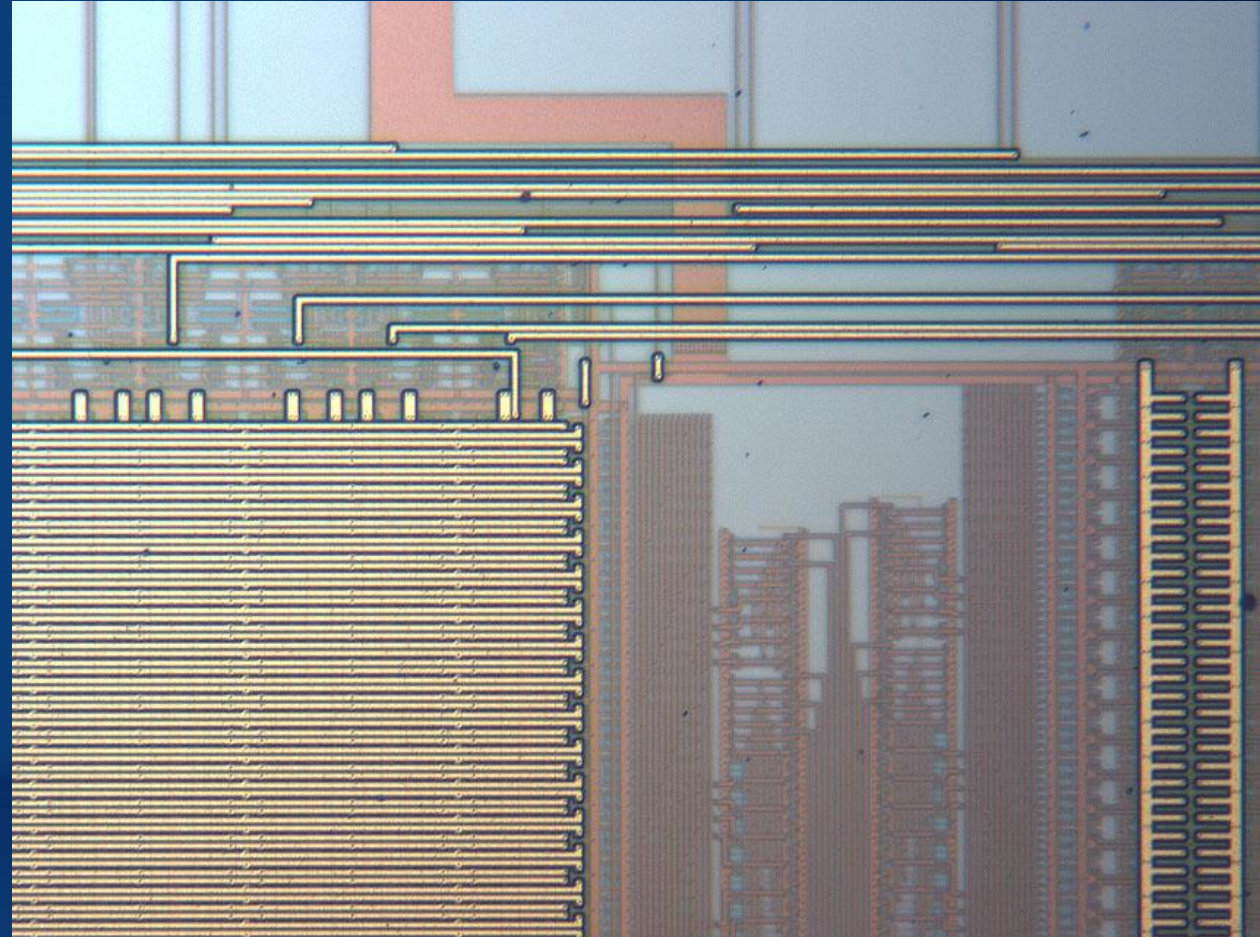
# NSF: Beyond the Current Roadmap...

- We see a full-stack “seismic shift”: America needs to invest in new materials, new materials processing and characterization, new fab, new devices and systems, and new computing, sensing, and communication systems answering both near-term supply chain concerns and longer-term Post-Moore challenges
- Furthermore, improving semiconductor fabrication foundry access for NSF-funded researchers would be a real difference-maker for our research communities



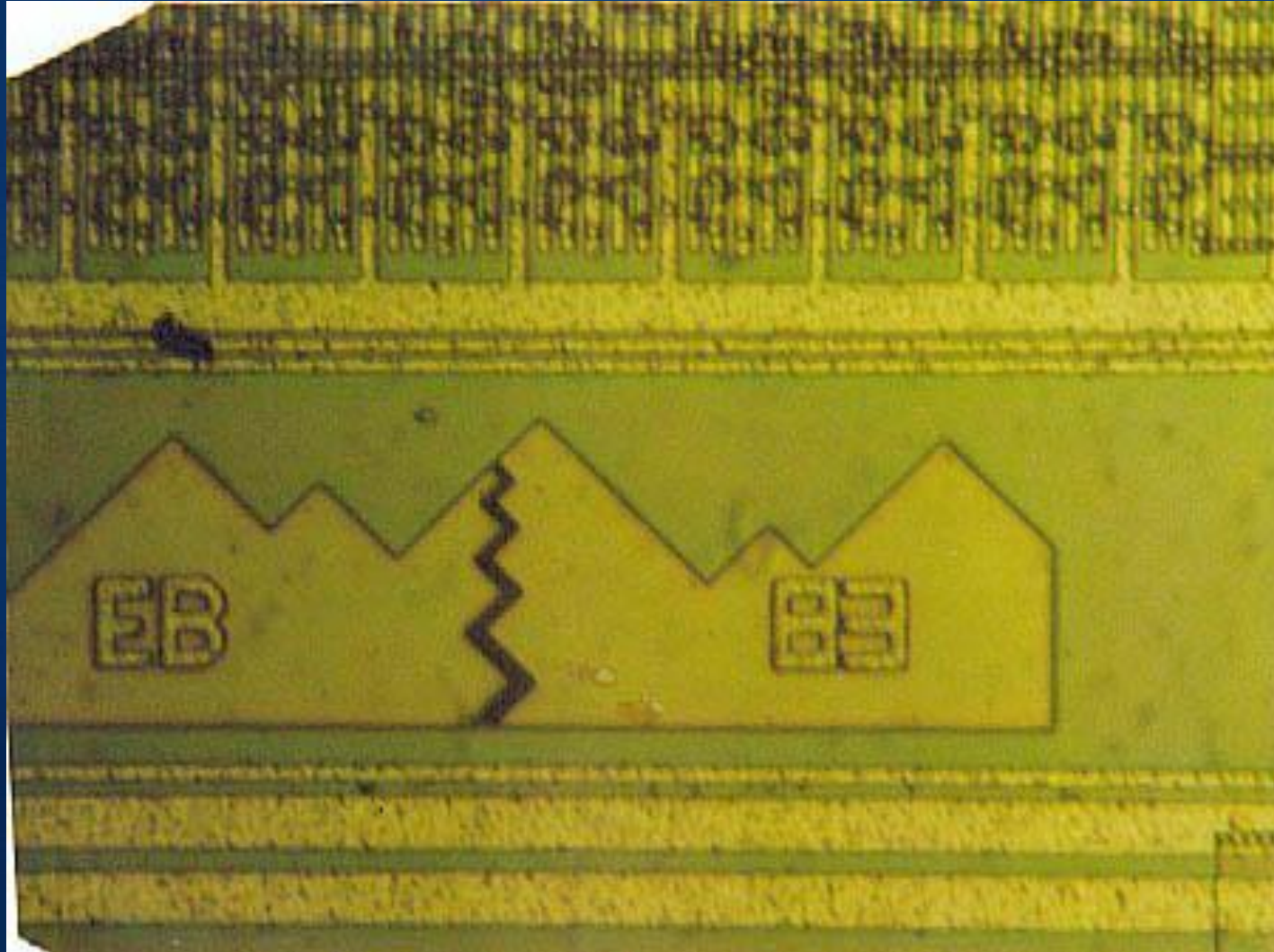
# Revitalization? What has changed?

- In my academic career, I designed, fabbed, and tested chips at every stage of my university experience
- When I started teaching the Digital VLSI course at the University of Utah in the 1990's, I kept up this tradition for my students
- But, it seems that this infrastructure (for both research and education) has degraded...



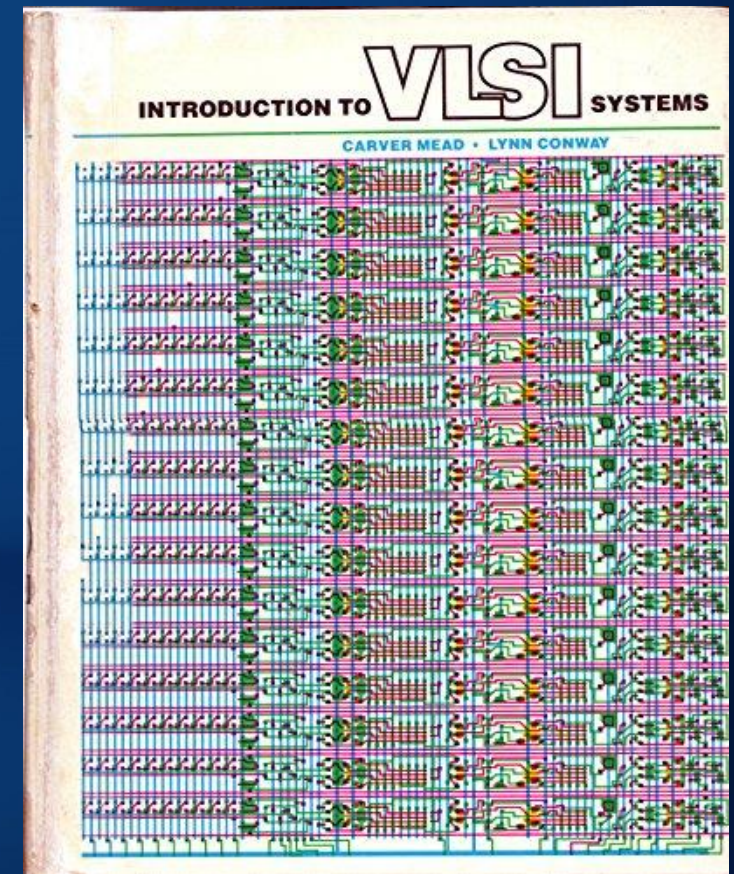


# My first chip...



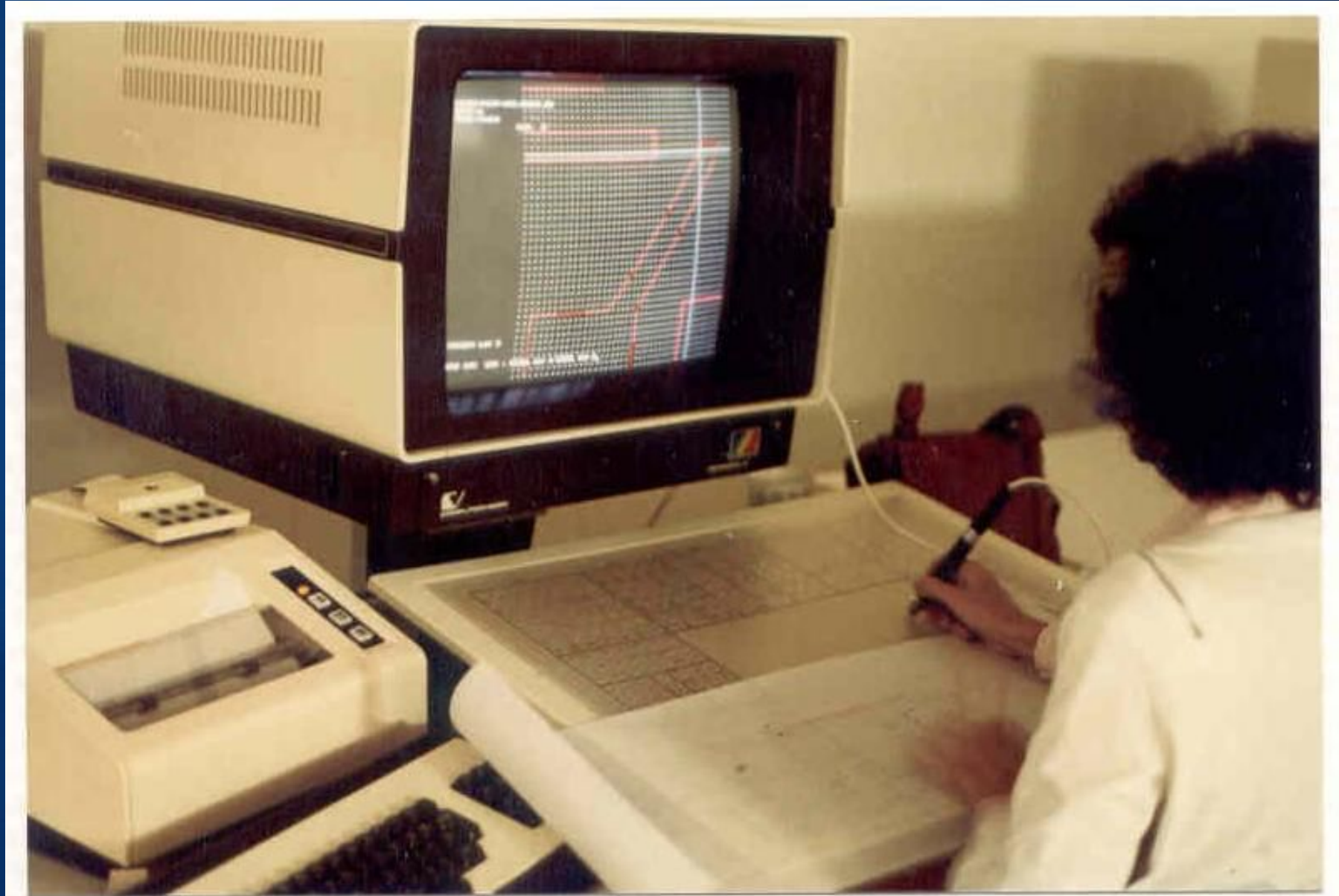
Polaroid photo taken  
Through the microscope  
Hood attachment

Some sort of nMOS process

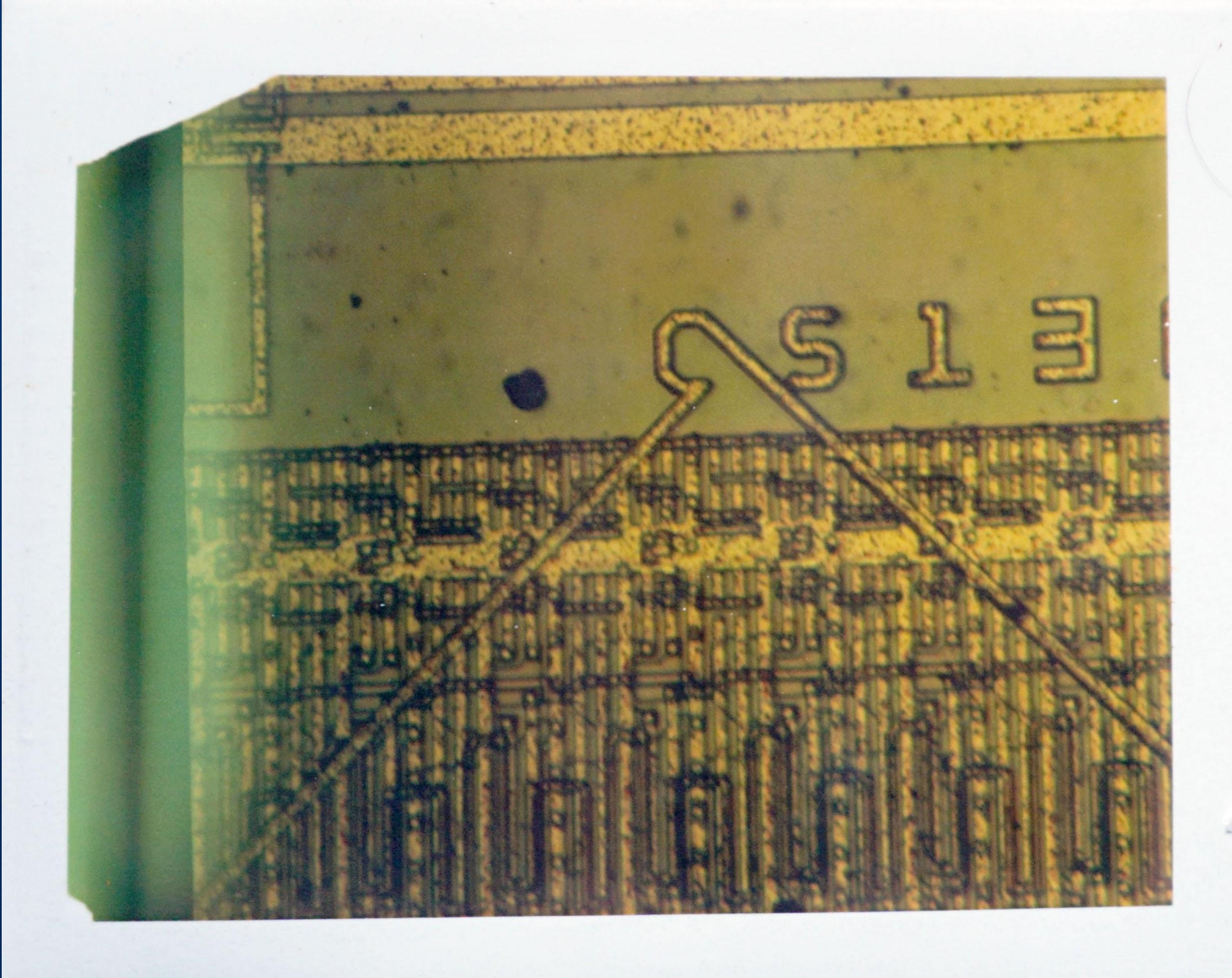




# Designed using a ComputerVision design system



# My first chip failure

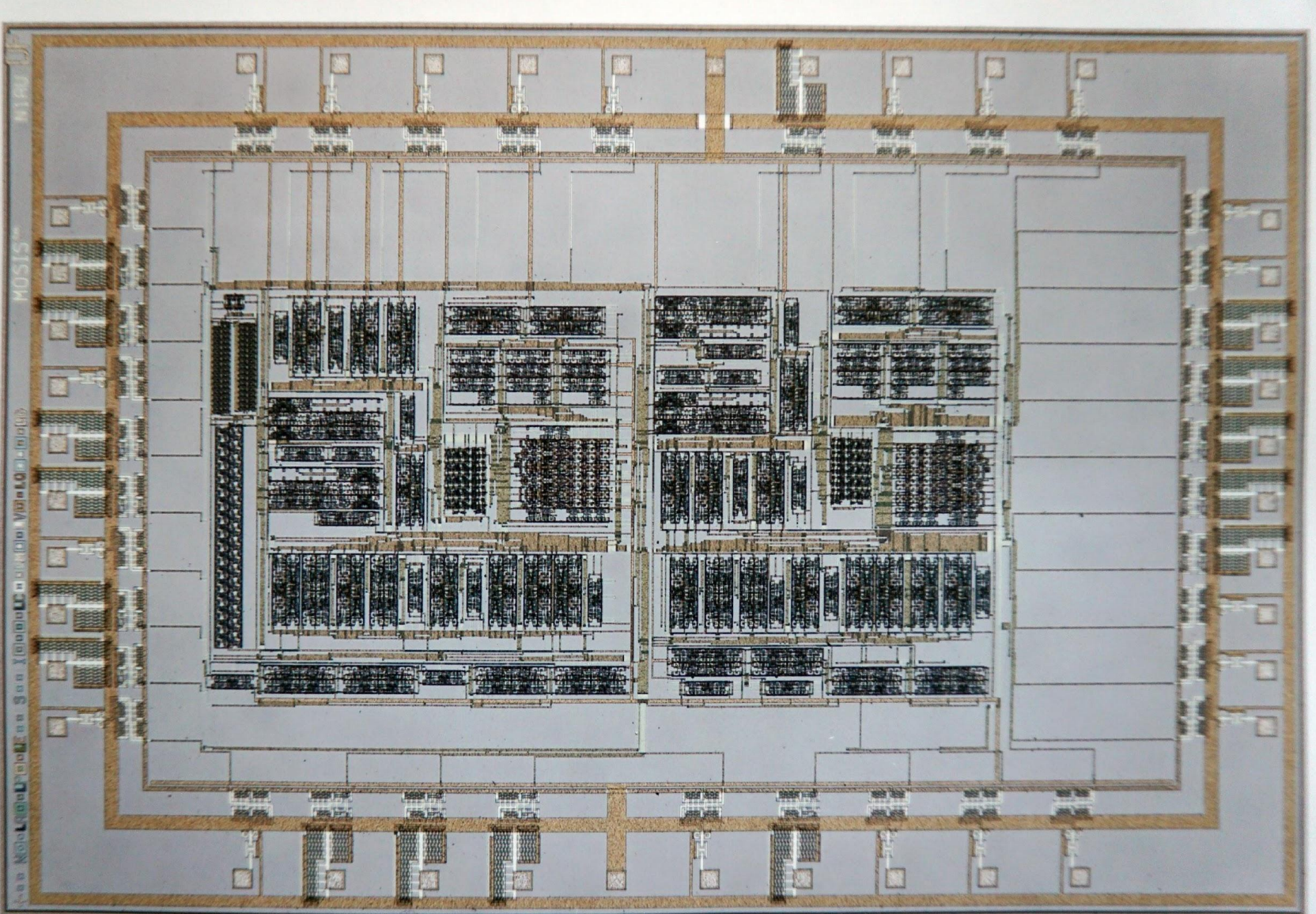


Some sort of rounding error in the program I used to generate the text

Looked fine on the CV display... Not so fine in the CIF apparently...



# Moving on – my PhD work at CMU circa 1989



Designed using Magic  
and some sort of  
external frame buffer  
on a VAX

CMOS – probably  
5u? Maybe 3u?

Fabbed by MOSIS



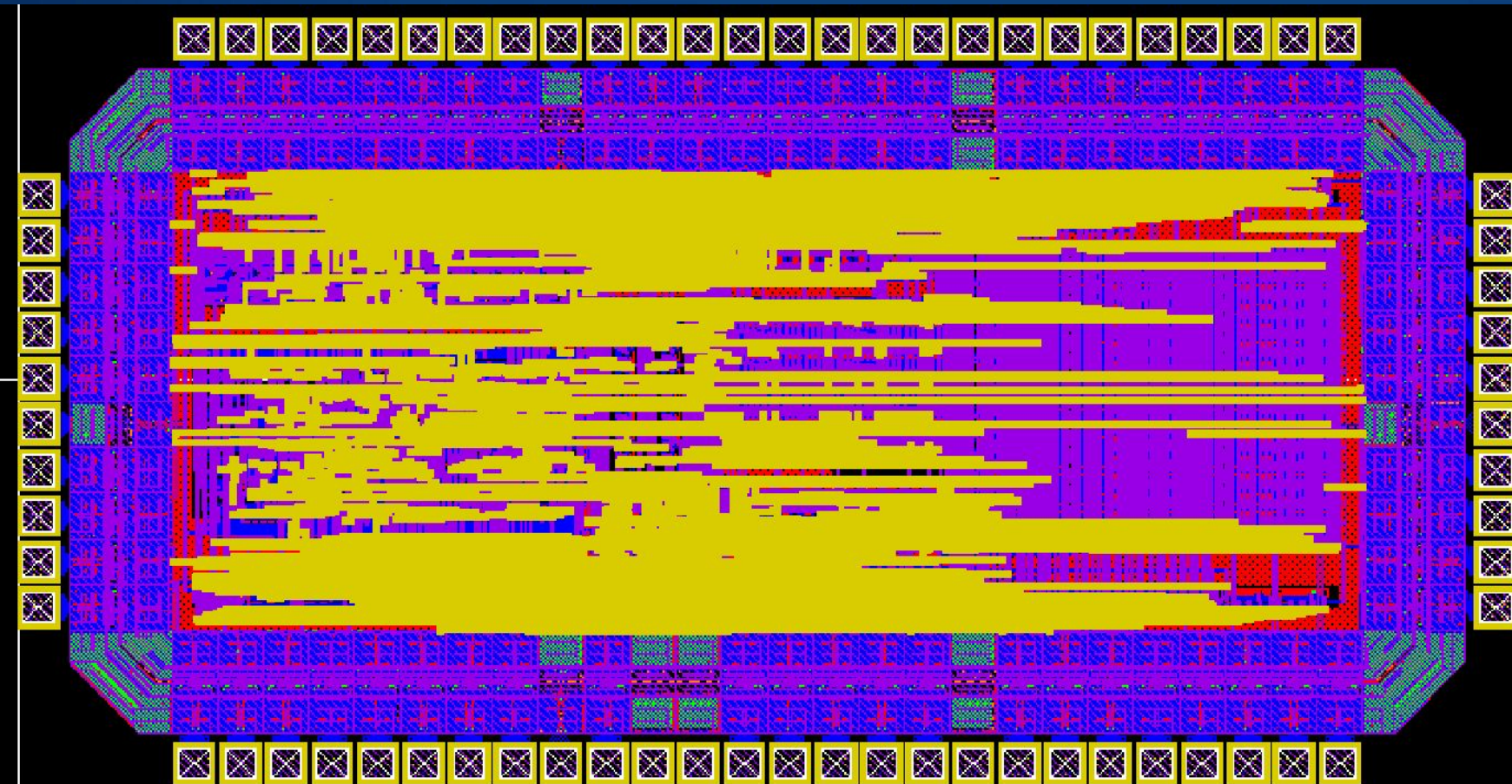
# Student designs at the University of Utah in the late 1990's to early 2000's

Now using Cadence and Synopsys

This example is a 16-bit processor – approx. 27k transistors

Using On-Semi 0.5u CMOS

Still fabbed through MOSIS





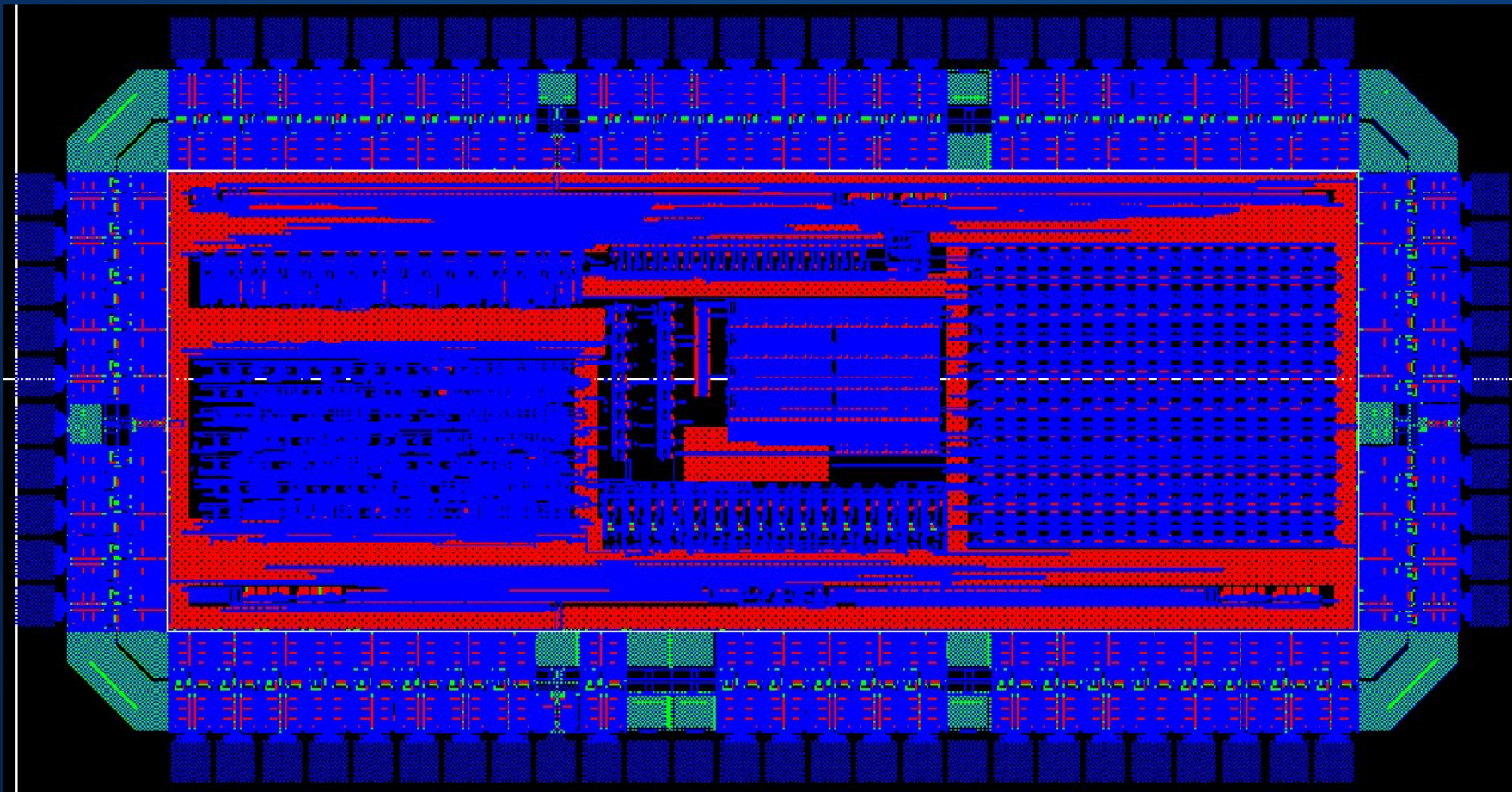
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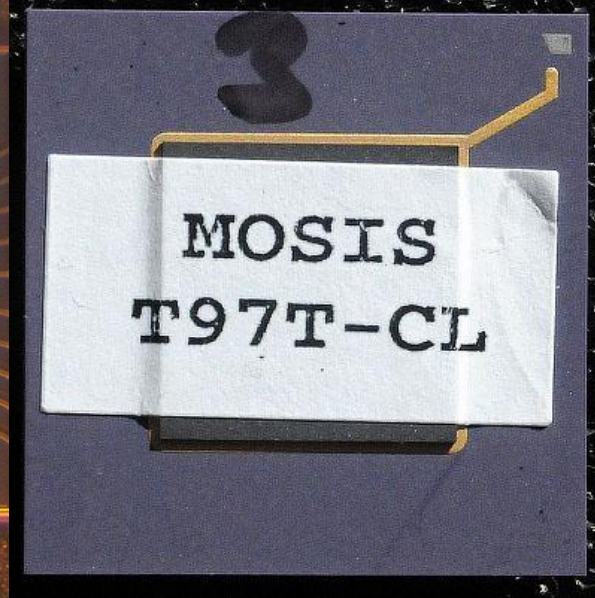
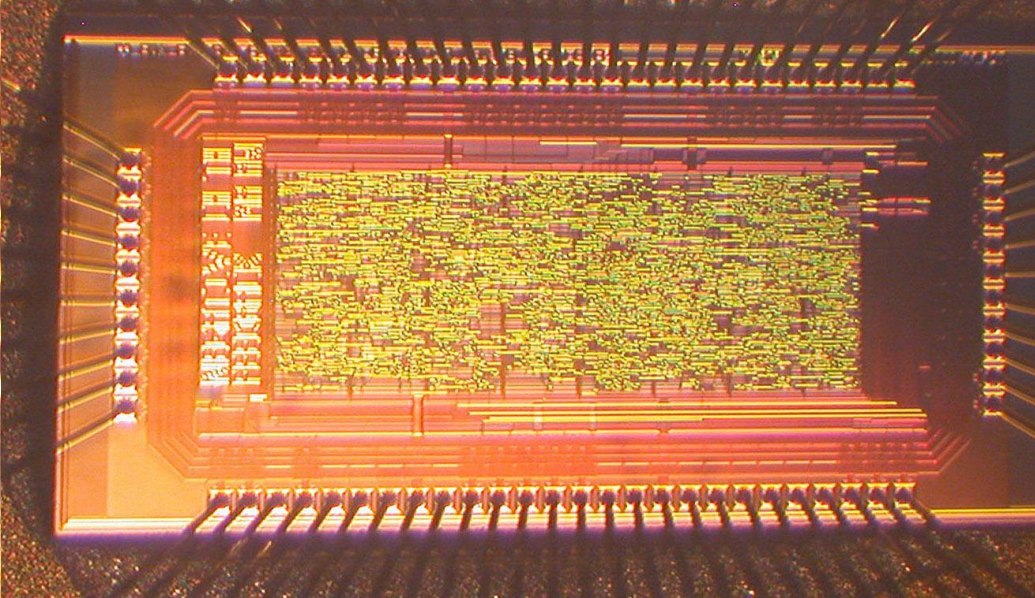
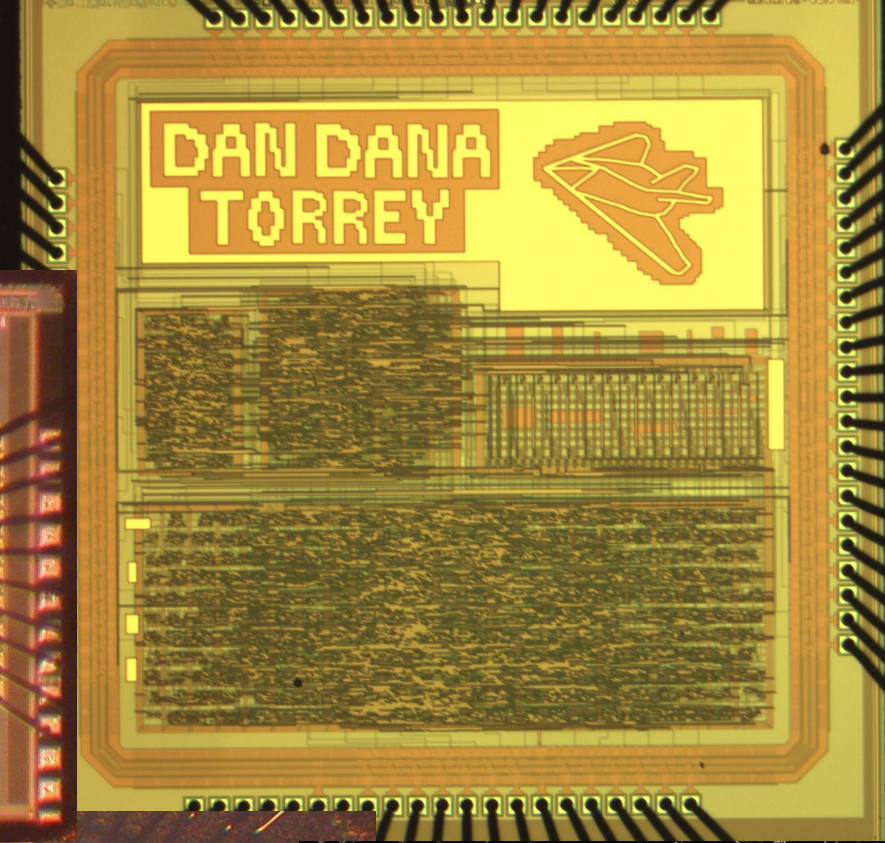
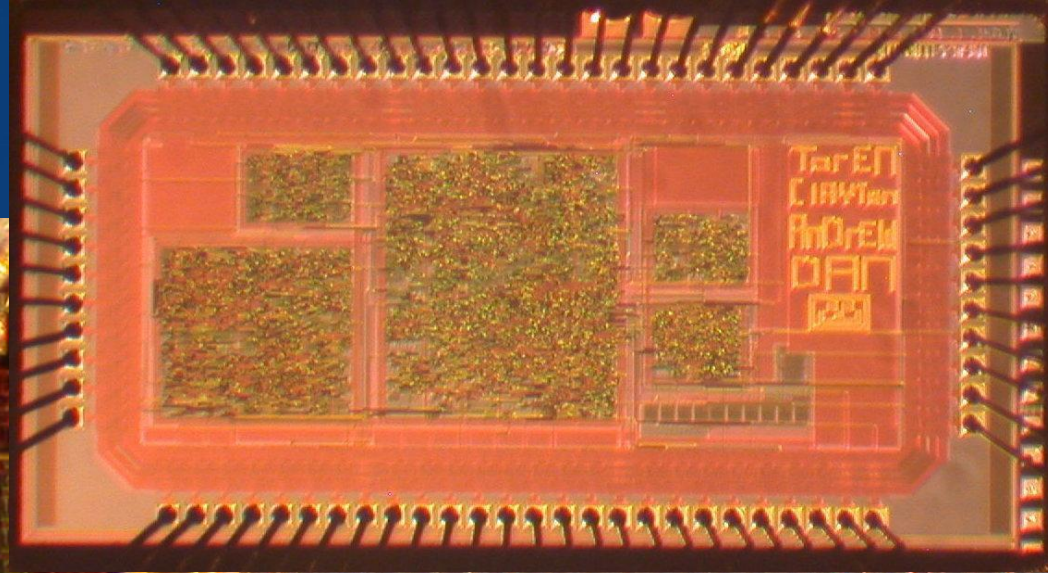
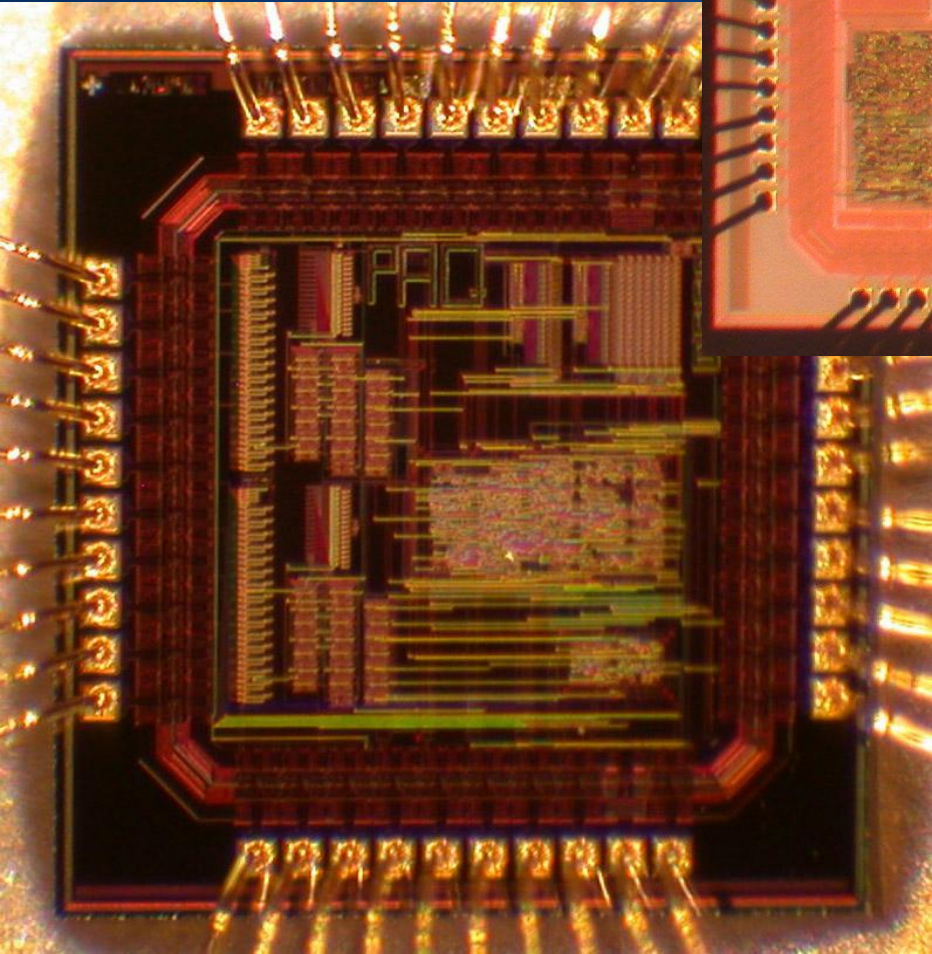
Using On-Semi 0.5u CMOS

Still fabbed through MOSIS





# More student designs...





# Along the way...

Digital VLSI Chip Design  
with Cadence and Synopsys  
CAD Tools



Erik Brunvand

I wrote a “lab manual” book describing how to use tools from Cadence and Synopsys, design your own cells, then use those cells in a CAD flow to get a chip fabbed through MOSIS...



# So what happened?

- Cutting edge fab becomes extremely challenging
- Cutting edge fab becomes extremely expensive
- MOSIS drops support for their University Program
  - Was using “friendly” legacy processes already
- Many classes start using FPGAs and HDL simulation
- Enrollments in old-school VLSI classes begins to wane...





# NSF RFI on semiconductor Research/Education

- Gauge the extent to which the community's research and educational agenda would be enabled by the availability of new or different resources, or the re-introduction of resources that were available in the past.
- Understand what specific activities the research community would pursue and how that activity would impact societal and national interests, if the impediments mentioned in the first category above are removed.





# NSF RFI on semiconductor Research/Education

- If you haven't already, please reply to this RFI!
  - **NSF.gov** – search for **CISE RFI Semiconductor**
- <https://www.nsf.gov/pubs/2021/nsf21112/nsf21112.jsp>
- <https://www.surveymonkey.com/r/CISERFIonSemiconductorResearchandEducation>





# On to the Workshop!

- I'm really looking forward to hearing what you all have to say!
- There are quite a few NSF program officers looking in too – there is a LOT of interest in this general area at the moment!
- Please make sure to speak up and join the conversation!

